(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No. 1 is Compulsory.

(2) Attempt any three questions out of the remaining five.

(3) Each question carries 20 marks and sub-question carry equal marks.

(4) Assume suitable data if required.

Q1. (a) Derive Poisson's and Laplace equation. (5)

(b) Explain boundary conditions of E and H fields for two media. (5)

(c) Explain the radiation resistance, directivity, Beam-width and directive gain of the antenna. (5)

(d) What is polarization? Explain all types of polarization. (5)

Q2. (a) Derive Maxwell's equations in integral and point form for static field. (10)

(b) State and Explain Poynting vector using modified Ampere's law, derive the pointing theorem and describe the significance of each of its terms. (10)

Q3. (a) Derive an expression for reflection and transmission coefficient for normal incidence in case of reflection from perfect dielectric. (10)

(b) Classify and Explain different types of wave Propagation and define the terms Critical frequency, Virtual height, Maximum unstable frequency and Skip distance. (10)

Q4. (a) Drive the expression for radiation resistance in far field region of an Infinitesimal dipole antenna. (10)

(b) Derive an expression for transmission line equation. (10)

Q5 (a) State Poynting Theorem and derive the expression for Poynting Vector. (10)

(b) Write a note on Smith chart and explain the steps to calculate SWR from the chart. (10)

Q6. (a) Write the generalized Maxwell's Equations in point form and integral form. (10)

(b) Explain the factors affecting the field strength of space wave signal. (10)

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Paper / Subject Code: 89364 / Embedded Systems and Real Time Operating Systems

TE/ETRX/SEM-VI/C-2019/DEC. 2022

(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. (a) Analyze the important issues faced during Hardware-Software Co-design. (5)
   (b) Compare White-Box and Black-Box testing. (5)
   (c) Draw program model CDFG control data flow graph to calculate the roots of quadratic equation. (5)
   (d) What is the Need of RTOS in Embedded system? (5)

2. (a) Draw and explain Waterfall Model used in Embedded Product Design Life-Cycle (EDLC) (10)
   (b) Demonstrate with examples Classification of embedded systems. Discuss various characteristics of the same. (10)

3. (a) Draw an architecture of the ARM Cortex-M3 and discuss its any three important features (10)
   (b) List and explain Design metrics of Embedded system with suitable graphs wherever necessary. (10)

4. (a) Discuss the differences between RISC and CISC cores. Which of them is used in the embedded systems? Why? (10)
   (b) Write in detail about types of memories required in the embedded system. (10)

5 (a) Compare i) RS-232, RS-485 ii) Bluetooth, Zig-Bee. (10)
   (b) Analyze the significance of Low Power modes in Cortex-M3 (10)

6. (a) Design Automatic Railway Ticket Vending Machine highlighting
      i. Specification requirements (choice of components),
      ii. Hardware architecture
      iii. Software architecture (10)
   (b) Discuss with one example each following:
      i. Hardware testing tools
      ii. Software testing tools (10)

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Paper / Subject Code: 89361 / Basic VLSI Design

TE/ETRX/SEM-VI/C-2019/DEC. 2022

(03 Hours) **Total Marks (80)**

Note:

1) Question No 1 is Compulsory.
2) Answer any three from the remaining questions.
3) Assume suitable data wherever required

Q1. Solve **any four** of the following **(20)**

a. Compare Full Custom and Semi-Custom design.

b. Write short note on Static CMOS Design

c. Implement the function F= $\overline{((D+E+A).(B+C))}$ using standard CMOS logic

d. Implement 4 X 4 NAND based ROM array.

e. Write short notes on Sense Amplifier.

Q2.a Explain Constant Voltage and Constant Field Scaling in detail with their advantages and disadvantages. **(10)**

b. Explain CMOS inverter characteristics mentioning all regions of operation. **(10)**

Q3.a Compare Pass transistor logic, NMOS logic and CMOS logic. **(10)**

b. Explain read and write operation of 1 T DRAM cell. **(10)**

Q4.a What are the drawbacks of dynamic CMOS logic? Show the modification in dynamic CMOS logic to overcome its drawback. **(10)**

b. Calculate noise margin of a CMOS inverter with the given parameters: **(10)**
NMOS $V_{TO,n}$ =0.6V, u_nC_{ox} = 60 uA/V^2, (W/L)n = 8,
PMOS $V_{TO,p}$ = -0.7V, u_nC_{ox} = 20 uA/V^2, (W/L)p = 12,
V_{DD} =3.3 V.

Q5.a Draw JK flip flop using CMOS and explain the working. **(10)**

b. Draw Carry Look Ahead Adder chain using Dynamic CMOS Logic. **(10)**

Q6. Solve **any 4 out of 5** carry equal marks **(20)**

a. Channel Length Modulation

b. Noise Margin

c. Pseudo -n-MOS

d. 4 X 4 Barrel Shifter

e. Flash Memory

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Duration 3 Hours **[Maximum Marks 80]**

NOTE:-1) Question 1 is **compulsory**
2) Solve **any three** from the remaining five questions
3) Assume suitable data if necessary.
4) Figures to the right indicate full marks

Q.1. a. Explain the concept of logistic regression. **20**

b. Explain the use of entropy while forming a decision tree.

c. List and explain in short design steps of forming a machine learning model.

d. Explain the terms: hyper plane, support vector that are used in SVM**.**

Q.2. a. Explain different error measures used for performance of regression. **10**

b. Explain the concept of under fitting and over fitting and perfect fitting with suitable diagrams. How to avoid under fitting and over fitting? **10**

Q.3. a. Explain the difference between linear regression and multiple regression? How will you compute cost function in linear regression? **10**

b.Find a linear regression equation for the following data: **10**

x	2	4	6	8
y	3	7	5	10

Q.4. a. Explain the steps used in forming Classification and Regression Trees. **10**

b. Explain Baye's theorem. Give suitable examples. **10**

Q.5. a. Explain Quadratic programming solution to find maximum margin separator. **10**

b.What are different kernels used for learning non-linear functions? **10**

Q.6. a.What is expectation maximization algorithm? Explain how it works for estimating the model parameters . **10**

b. Explain the steps involved in developing the ML model for Credit card Detection. **10**

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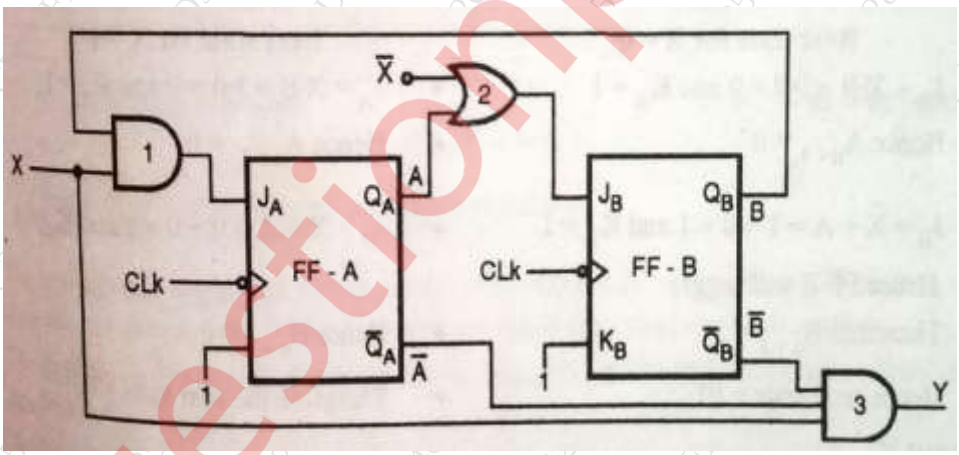
Time: 3 Hrs **Max. Marks: 80**

N.B.: - (1) Question number 1 is compulsory.

(2) Solve any Three from remaining five questions.

(3) Draw neat logic diagram & assume suitable data whenever necessary.

Q.1	**Solve any four**	**Marks**
a	List any six features of VHDL.	05
b	Differentiate between Mealy and Moore machine.	05
c	Write a VHDL code for Half adder circuit.	05
d	Explain Booth's multiplication with example.	05
e	Write a short note on Register transfer level (RTL).	05
Q.2		
a	Analyze the sequential circuit shown below. Hence derive the state table and state diagram.	10



b	Write a VHDL code for JK flip flop	10
Q.3		
a	Design a Mealy sequence detector circuit to detect an overlapping sequence "1010" using D flip flop and logic gates.	10
b	Write a VHDL code for Traffic light controller system.	10
Q.4		
a	Write a VHDL code for 4 bit UP-DN counter using asynchronous reset.	10

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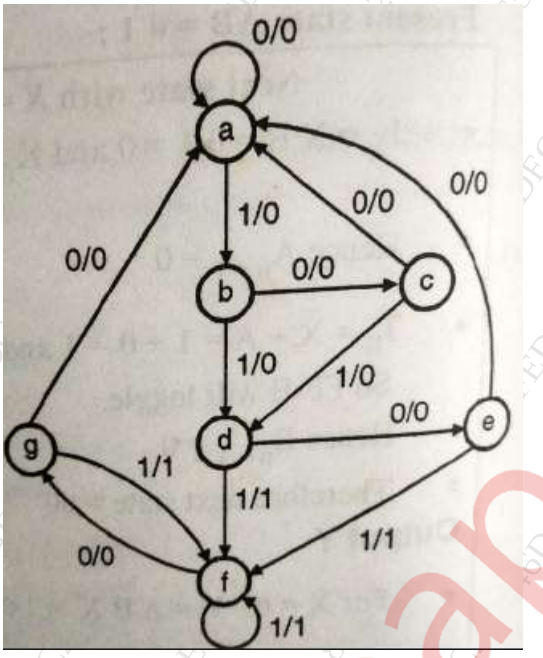
b For a given state diagram obtain a reduced state diagram using state reduction technique. 10



Q.5

a List the features of XC4000 FPGA family and discuss it with the help of neat block diagram. 10

b Write a VHDL code for Booth's multiplier. 10

Q.6 Solve any Four

a Write a short note on different modelling styles used in VHDL. 05

b List the features of complex programmable logic devices. 05

c Write a VHDL code for 2-bit parallel multiplier in data flow modelling. 05

d Write a short note on functional and timing simulation. 05

e Explain VHDL operators with example. 05

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