(Sem-VII (Old)) / ETRX / Power Electronic & Drives / May-16.

QP Code : 29832

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question **No. 1** is **compulsory**.
(2) Solve **any four** questions out of remaining **six** questions.
(2) **Figures** to the **right** indicate **full** marks.

1. (a) What do you understand by subsynchronous speed and super-synchronous speed of Ac motor. **5**
(b) Differntiate between voltage source invester and current source invester. **5**
(c) Explain class A chopper and derive the relation for o/p voltage. **5**
(d) Explain the need of harmonic reduction in inverter. **5**

2. (a) What do you understand by dual converter. Explain it with the help of circuit diagram and waveforms. **5**
(b) Explain multiple PWM to control the output voltage in investers. How it reduces harmonics present in the o/p. **5**

3. (a) Draw and explain voltage commutated chopper with the help of waveforms. **10**
(b) Draw and explain off-line ups and on-line ups. State advantages and dis-advantages of each type. **10**

4. (a) Explain Basic series invester wish the help of circuit diagram and wave forms. **10**
(b) With the help of block schematic explain v/f control scheme to control the speed of three phase induction motor. **10**

5. (a) For a current commutated chopper, peak commutating current is thrice the maximum possible load current. The source voltage is 220V dc and main SCR turn-off time is 20μs. For a maximum load current of 180A, Compute, **10**
(a) The value of commutating components L and C.
(b) The maximum capacitor voltage.
(c) The Peak commutating current.

(b) Explain the rotor resistance control technique to control the speed of three phase induction motor. **10**

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6. (a) Explain the working of flyback converter in dis contineous and contineous current mode. Draw waveforms.
   (b) Explain the effect of source inductance in fully controlled bridge converter with R-L load. Derive the relation for load voltage and load current.

7. Write short notes on
   (i) Class E chopper 7
   (ii) Slip Power recovery scheme 7
   (iii) Slip-torque curve of induction motor. 6

SEM VII (OLD) - ETRX

VLSI DESIGN MAY'16

QP Code : 29908

(3 Hours) [Total Marks : 100

N.B.- (1) Question No. 1 is **Compulsory.**
(2) Attempt any **Four** out of remaining **six** questions.
(3) Assume **suitable** data wherever **necessary.**

1. Answer any **FOUR.** (20)
   (a) Define threshold voltage of an enhancement and depletion type MOSFET. What is the effect of substrate bias on threshold voltage of the device?
   (b) Differentiate between the process of ion implantation and diffusion in fabrication of a MOS transistor.
   (c) Construct a 2 X 2 array multiplier circuit and write a verilog module for your design.
   (d) Find the flat band voltage of a MOS capacitor with substrate doping concentration of $10^{16}/cm^3$ and silicon dioxide thickness of 500A°. Assume $Q_{ox} = 10^{11} q/cm^2$ and $\varphi_{ms} = -1.1V$.
   (e) Explain the effect of full scaling and constant voltage scaling on current density and delay in a MOSFET.

2. (a) Assuming that the work function of the metal is smaller than that of the p-type semiconductor, pictorially depict for an n-channel MOS transistor, the energy bands and Fermi level in the semiconductor, conduction band in the oxide, Fermi level in metal under the following conditions : (10)
      i. Flat band condition
      ii. Onset of inversion at the surface.
      iii. When the surface is depleted of carriers.
      iv. When the metal and semiconductor are shorted.
   (b) An enhancement mode n-channel MOSFET has the following parameters. (10)
   Threshold voltage $V_T = 0.8$ V, Channel length modulation coefficient $\lambda = 0.05/V$, $\mu_n C_{ox} = 20\ \mu A/V^2$, $W/L = 20$
   Find the drain current for the following cases.
      (i) $V_g = 5$ V, $V_D = 4$ V, $V_S = 2$ V
      (ii) $V_g = 2.8$ V, $V_D = 5$ V, $V_S = 1$ V

3. (a) What do you mean by inverter ratio? Derive the same for depletion load nMOS inverter which is driven by another similar inverter. (10)
   (b) Implement the following Boolean function in CMOS logic: (10)
   $$Y = \overline{(AB + AC) + (AD)}$$
   Draw the optimized stick diagram of the logic gate using Euler path.

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4. (a) An nMOS transistor is to be fabricated. Describe its fabrication steps giving the mask sequence. Sketch the masking steps in cross-section view. (10)
   (b) Sketch and explain the CV characteristics of MOS capacitor with n- type substrate under low frequency conditions. How does the characteristic change under high frequency condition? (10)

5. (a) Draw the schematic diagram, stick diagram and mask layout of a CMOS inverter using λ based design rules. (10)
   (b) Implement a 2:1 multiplexer circuit using CMOS transmission gates. Write a Verilog module for the circuit at switch level of abstraction. Write a test bench to check the functionality of the circuit. (10)

6. (a) Explain various sources for power dissipation in digital CMOS circuit. (10)
   (b) Draw the p-well CMOS inverter and explain the latch up effect in it. What are the remedies to avoid the latch up problem in the circuit? (10)

7. Write short notes on any **two**:
   (a) Short channel effects
   (b) Design rules and their necessity
   (c) Comparison of types of loads in NMOS inverters (20)

FILTER DESIGN

QP Code : 29694 MAY '16

(3 Hours) [Total Marks: 100]

N.B.: (1) Question No. 1 is compulsory.
(2) Attempt any four questions from remaining six questions.
(3) Assume suitable data if necessary.
(4) Figures to the right indicate full marks.

1. Answer the following **20**
   (a) Compare Butterworth, Chebyshev, Inverse Chebyshev and Elliptic filters.
   (b) Prove that the symmetrical FIR filters have linear phase characteristics.
   (c) Justify why ideal filters are not realizable.
   (d) Explain the concept of inductance simulation.

2. Design digital Chebyshev filter to meet the following specifications **20**
   Pass-band ripple ≥ 0.89
   Pass-band edge ≤ 1.5 KHz
   Stop-band attenuation ≤ 0.003
   Stop-band edge ≥ 4 KHz
   Sample rate: 10 KHz
   Use Bilinear transformation

3. (a) Derive the relation for order of filter and cutoff frequency for Butterworth filter. **10**
   (b) Explain Gibb's phenomenon. State its significance. **10**

4. (a) Design digital FIR filter for the following specifications **12**
   $$|H_d(e^{jw})| = 2e^{-j5w} \quad for\ |w| \leq 0.5\pi$$
   $$= 0 \quad otherwise$$
   (b) What is FDNR? State its properties. **08**

5. (a) Explain frequency warping effect in Bilinear transformation technique. **10**
   (b) What is adaptive filter? Explain the need of adaptive filter in signal processing. **10**

6. (a) Explain Leapfrog realization technique in detail. **10**
   (b) Explain MMSE criteria in adaptive filter **10**

7. Write short notes on (Any two) **20**
   (a) Frequency sampling technique.
   (b) Analog frequency realization
   (c) Quadrature mirror filtering.

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