BE - Sem-VIII - ETRX – Advanced VLSI Design.
(Rev.)

Q.P. Code : 8014

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. 1 is compulsory.
(2) Answer **Any Four** questions out of remaining questions.
(3) Assume any suitable data wherever required.

1. a) Explain Charge sharing and charge leakage problem of dynamic Logic circuit. **5**

b) Explain cross talk in integrated circuits. **5**

c) Explain EEPROM using floating gate NMOSFETS. **5**

d) Compare clock skew and jitter. **5**

2. a) What is effect of interconnect parasitic on delay? How delay can be reduced ? What is Elmore delay model? **10**

b) Give and explain single phase clock system and explain its drawback. **10**

3. a) Implement 4 bit adder using Carry Look Ahead (CLA) principle. **10**

b) State the need of input and output circuit. Explain with neat diagram the schematic and design considerations for the same. **10**

4. a) Explain frequency compensation in operational amplifier. **10**

b) Implement the following function using NOR-NOR implementation for a PLA. **10**
F1= abc+ a'b'c'
F2= a'c' + a'b
F3= ab' +ac

5. a) What are the different clock generation schemes employed in VLSI systems. Discuss 'H' tree clock distribution in high density CMOS circuits. **10**

b) Draw schematic for 6T SRAM cell and explain its stability criteria. Also draw and discuss its butterfly curve. **10**

6. a) Draw 4x4 NOR based ROM array circuitry stored following data 1011,1001,0101,0011. 10

b) Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. 10

Q7. Write short notes on (any three) 20

a) Low power design consideration.
b) Carry skip adder.
c) Interconnect scaling.
d) Switched capacitor circuit.

BE- Sem- VIII - Rev - ETRX - Robotics & Automation

QP Code : 8152

(3 Hours) **[Total Marks : 100**

N.B.:
(1) Question No.1 is compulsory.
(2) Attempt any four questions out of remaining six questions.
(3) Assume suitable data wherever required.

Q.1. a) Define hard/fixed, soft/ flexible automation and hence the relative cost effectiveness of different types of automation with a neat sketch. [5]
b) How are robots classified? [5]
c) With neat sketch define the Joint and Link parameters [5]
d) Explain how parabolic blends eliminate infinite acceleration points on the trajectory of robots. [5]

Q.2. a) Find the joint position of the tool tip of the Adept One robot when the joint variables are $q = [\Pi/4, -\Pi/3, 120, \Pi/2]^T$
Where $d = [877, 0.0, d3, 200]^T$, $a = [425, 375, 0.0, 0.0]^T$ [10]
b) Explain the basic steps involved in bounded deviation algorithm for straight line motion . [10]

Q.2. a) Explain the conditions for the existence of the Inverse Kinematics solutions and how are they simplified for the model robot with a spherical wrist . [5]
b) How do you find the inverse kinematics solutions based on the numerical and analytical approaches ? [5]
c) Explain Trajectory planning with examples. [10]

Q.3. a) What are the considerations for applying DH algorithm? Explain the direct kinematic solution for a three link planar Robot. [10]
b) Explain noise in images. How are these classified? [10]

Q.4 a) Explain shrink and swell operators with examples. How are these applied? [10]
b) Name and explain with diagrams all the lower kinematic pairs. Indicate those that cannot be used in an actuated Robot joint and the reason for it. [10]

Q.5. a) What are the important edge detection methods for polygonal objects? Explain one of the edge detection technique? [10]
b) What are area descriptors? What are its advantages over line descriptors? Explain the different moments to characterizing shape? [10]

Q.6 a) Explain the basic steps involved in bounded deviation algorithm for straight line motion . [10]
b) Draw & Explain the Ladder Diagram for controlling lubricating oil being dispensed from a tank [10]

Q.7. Write notes on the following [20]
(a) Robot specification (b) Template matching in Robot vision
(d) Task planner simulation (e) Link co-ordination arm equation

XXX

RJ-Con. 10530-15.

B E Sem VIII (R) 2015, Embedded System & Real Time Programing
Branch :- Electronics.

QP Code : 8306

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. 1 is compulsory.
(2) Answer any four of the remaining six questions.
(3) Draw neat diagram and assume suitable data wherever required.

1. (a) Explain low power modes of MSP430 with the help of clock modules. 5
(b) What are the challenges in meeting various design metric/requirements. 5
Explain for :
(i) Low power
(ii) High performance
(c) Explain serial communication SCI & SPI, compare the same. 5
(d) Compare various scheduling policies. 5

2. (a) Explain parallel peripherals of MSP430 10
(b) Explain CAN features and protocols. 10

3. (a) Explain various modifiers and their purpose and use in an embeded system. 10
(b) Compare assembly language programming with c-programming. 5
(c) Compare ARM state with THUMB state. 5

4. (a) Explain interrupts/exceptions and its handling in ARM. 5
(b) With the help of suitable diagram give difference between RS485 and RS232, also compare its characteristics, features. 10
(c) Compare, explain various operating modes of ARM. 5

5. (a) In a real time system having periodic Tasks T_1, T_2, T_3 and aperiodic task T_4 all requesting at time t = 0 having following properties. 10

Task	Period	Execution time	Deadline
T_1	210	70	210
T_2	70	21	70
T_3	140	28	140
T_4	aperiodic	80	420

[TURN OVER

5. (a) What is Hopfield model of neural network. Explain its algorithm and energy minimization in auto - associative Hopfield network. 1
   (b) Expalin RBF network and compare it with MLP. 1

6. (a) Explain the operation of fuzzy logic control with process inference block. 1
   (b) Explain Kohonen's Self Organizing Learning Algorithm. 1

7. Write short note on : 20
   (a) LMS Algorithm
   (b) Neurofuzzy controller
   (c) Brain state in box model
   (d) Simulated annealing.

BE- Sem-VIII – ETRX – DSP Processors & Architectures

QP Code : 8085

Duration: **Three** Hours | Total Marks: **100**

Instructions to candidates
1. Question No. 1 is Compulsory.
2. Attempt any **Four** questions from remaining six.

10	1.	Answer the following: (**Any Four**)	20
	a.	Write a subroutine program to explain bit-reversed addressing.	
10	b.	Explain in-place computation in FFT algorithm.	
	c.	Explain the features of a program sequencer unit of a programmable DSP.	
10	d.	Differentiate between MAC and MACD instructions by the way of explaining them.	
10	e.	What are the various classes of interrupts available in TMS320C54XX processor?	
	2. a.	Explain the pipeline operation with branch and call instructions in C5X. Why it requires four clock cycles for program control transfer?	10
20	b.	Explain PMST register in C54X.	10
	3. a.	Explain with suitable examples addressing modes of TMS320C54X.	10
	b.	Discuss the techniques used in DSP architecture to increase the speed of operation and operations that should be accomplished in single clock to achieve parallelism in DSP implementation.	10
	4. a.	Explain with block diagram, internal architecture of TMS320C62X processor.	10
	b.	Explain the process of interpolation and decimation in brief.	04
	c.	Explain the implementation of 8-tap FIR filter using MAC units.	06
	5. a.	Compare the features of TMS320C5X and TMS320C54X.	10
	b.	Explain the architecture of ADSP-21XX with suitable diagram.	10
	6. a.	Let the value of DP and ARP be 8 and 2 and the content of AR2 and BMAR be 2800h and 2900h respectively. Specify the addressing modes and the addresses for the source and destination for the following instructions: BLDD #400, 25h BLDD #400h, *+ BLDD 45h, #450h	6
	b.	What is ARAU, INDX and ARCR in C5X processor?	6
	c.	Explain on-chip peripherals of C5X DSP.	8
	7. a.	Write an assembly language program of TMS320C54XX processor to compute the sum of three product terms given by the equation, $y(n)= h(0)x(n) + h(1)x(n-1) + h(2)x(n-2)$ with usual notation. Find y(n) for signed 16 bit data samples and 16 bit constants.	10
	b.	Explain the implementation of adaptive filter for the implementation of basic DSP algorithms.	10

RJ-Con. 9881-15.