13/14 INST/Sem-III (CBSQS)/Electrical Networks Analysis 8 Syntesis

Q.P. Code: 5256

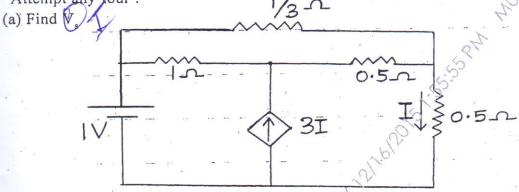
(3 Hours)

[Total Marks: 80

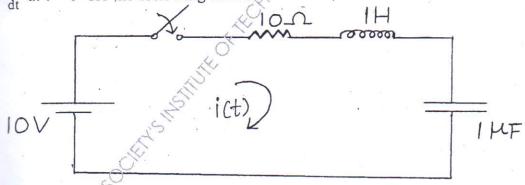
N.B.: (1) Question No.1 is compulsory.

- (2) Answer any three out of remaining questions.
- (3) Assumptions made should be clearly stated.

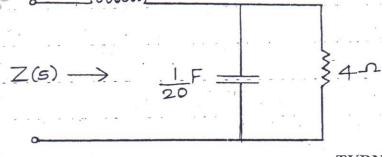
1. Attempt any four:



(b) Switch is closed at t = 0. Assuming all initial conditions as zero, find i and  $\frac{d\mathbf{t}}{dt}$  at  $t = 0^+$  for the following network.



Determine Z(s)-in the network. Find poles and zeros of Z(s) and plot them on s-plane.



MD-Con. 11523-15.

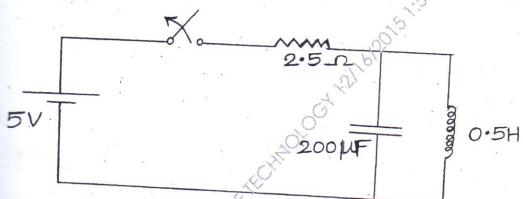
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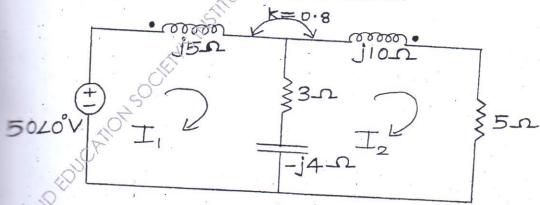
(d) Test whether the following polynomials are Hurwitz.

(i)  $P(s) = (s^2 + (s^3) + 3(s^2) + (2x) + 12$ (ii)  $P(s) = s^4 + 7s^3 + 6s^2 + 21s + 8$ (e) Using the relation Y = Z-1, show that  $|z| = \frac{1}{2} \left( \frac{z_{22}}{y_{11}} + \frac{z_{11}}{y_{22}} \right)$ 

2. (a) Exthe network shown below, switch is opened at t = 0. If steady state is attained before switching, find the current through



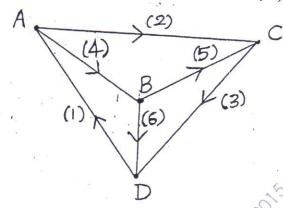
(b) Find voltage across  $5\Omega$  resistor using mesh analysis.



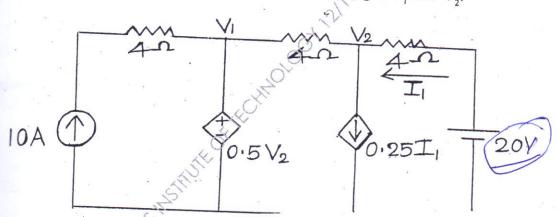
MD-Con. 11523-15.

3. (a) For the following graph of the network, write.

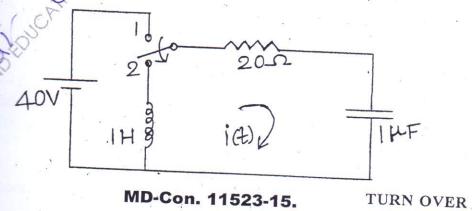
Incidence Matrix, (ii) Tieset Matrix and (iii) Cutset Matrix



(b) Using Superposition Theorem, determine the voltages  $V_1$  and  $V_2$ .

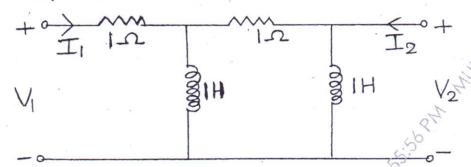


In the following network, switch is changed from position 1 to 2 at t = 0. Before switching, steady state condition has been attained.



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(b) Find Z parameters for the network.

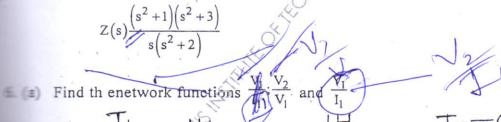


5. (a) Test whether the following functions are positive real-

(i) 
$$F(8) = \frac{s^2 + 6x + 5}{x^2 + 9s + 14}$$

(ii) 
$$F(s) = \frac{s^2 + 1}{s^3 + 4s}$$

(b) Realize Foster I and Foster II forms of the following impedance function.



Find th enetwork functions  $V_1$  and  $V_2$  and  $V_3$   $V_4$   $V_4$   $V_4$   $V_4$   $V_5$   $V_6$   $V_7$   $V_8$   $V_8$ 

Find Cauer I and Cauer II forms of RL impedance function.

$$Z(s) = {2(s+1)(s+3) \over (s+2)(s+6)}$$

## S.E./Sem-III /Rev. 2012/ CBSGS/ INST. / Nov. 2015/ Analog Electronics.

QP Code: 5214

(3 Hours)

[ Total Marks: 80

20

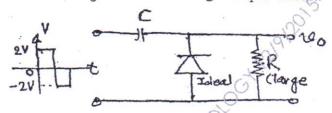
N. B.: (1) Question 1 is compulsory.

- (2) Attempt any four from remaining five questions.
- (3) All questions carry equal marks.
- (4) Assume suitable data wherever necessary.
- 1. Attempt any five :-

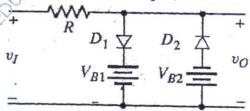
(a) Calculate the CMRR (in dB) for the circuit measurements of  $V_D$  = 1 mV,  $V_{O-D}$  = 120 mV, and  $V_{CM}$  = 1 mV,  $V_{O-CM}$  = 20 uV.

(b) For an op-amp having a slew rate of  $SR = 2.4 \text{ V/}\mu\text{s}$ , what is the time taken for output to change from -15 V to +15 V.

(c) Determine V<sub>O</sub> for the following clamper circuit.



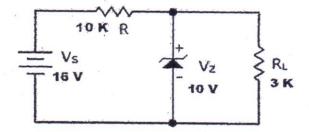
- (d) Given I<sub>DSS</sub> = 16 rnA and V<sub>P</sub> = -5 V, sketch the transfer characteristics using the data points. Determine the value of I<sub>D</sub> at V<sub>GS</sub>=-3 V from the curve, and compare it to the value determined using Shockley's equation.
- (e) Crossover distortion behavior is characteristic of Class A Power amplifier. State true or false with reason.
- (f) Compare class A, class B and class C power amplifier based on,
  - (a) Output waveform for collector current
  - (b) Linearity
  - (c) Distortion
  - (d) Efficiency
- 2 (a) Determine output voltage. Assume, V<sub>B1</sub> = 8 V, V<sub>B2</sub> = 6 V and input to be sine wave of 20 V peak.



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(b) For the Zener diode network, determine V<sub>L</sub>, V<sub>R</sub>, I<sub>Z</sub> and P<sub>Z</sub>. Consider supply voltage of 16 v, zener voltage of 10 V, series resistor of 10 K and load resistance of 3 K.





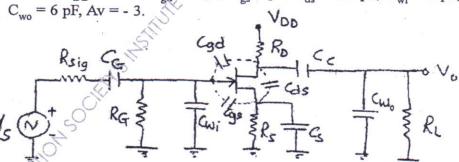
(c) Explain working of bridge rectifier.

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- 3. (a) Determine the levels of  $I_{CQ}$  and  $V_{CEQ}$  for the CE BJT amplifier with voltage-divider configuration. Consider  $R_1 = 82$  K,  $R_2 = 22$  K,  $R_C = 5.6$  K,  $R_E = 1.2$  K,  $V_{CC} = 18$  v and  $\beta = 50$ .
- Q

(b) Explain constructing and working of D-MOSFET.

- c 4
- (c) What is harmonic distortion? Write the equation for total harmonic distortion.
- 10
- 4. (a) Determine the higher cut off frequencies for the given circuit diagram. Given:  $C_G = 0.01 \, \mu\text{F}$ ,  $C_C = 0.5 \, \mu\text{F}$ ,  $C_S = 2 \, \mu\text{F}$ ,  $R_{SIG} = 10 \, \text{k}$ ,  $R_G = 1 \, \text{M}$ ,  $R_D = 4.7 \, \text{k}$ ,  $R_S = 1 \, \text{k}$ ,  $R_L = 2.2 \, \text{k}$ ,  $R_{DSS} = 8 \, \text{mA}$ ,  $V_P = -4 \, \text{V}$ ,  $rd = \infty$ ,  $V_{DD} = 20 \, \text{V}$ ,  $C_{gd} = 2 \, p\text{F}$ ,  $C_{gs} = 4 \, p\text{F}$ ,  $C_{ds} = 0.5 \, p\text{F}$ ,  $C_{wi} = 5 \, p\text{F}$ ,  $C_{wo} = 6 \, p\text{F}$ , Av = -3.



- (b) Derive equation for three Op Amp Instrumentation amplifier. Give advantages and applications of Instrumentation amplifier.
- (a) Draw and explain a series voltage regulator.

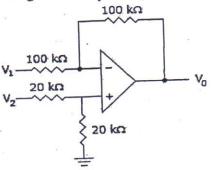
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(b) Explain integrator using Op Amp. Draw its frequency response. State
disadvantages of basic integrator and how it is overcome in practical
integrator circuit.

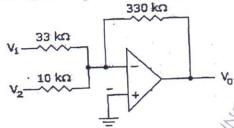
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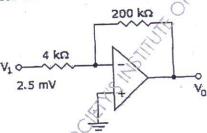
6. (a) Derive the expression for output voltage and hence determine the output voltage when  $V_1 = -V_2 = 1$  V.



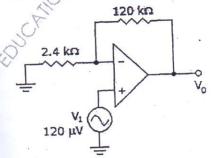
(b) Derive the expression for output voltage and hence calculate the output voltage if  $V_1 = -0.2 \text{ V}$ ,  $V_2 = 0.1 \text{ V}$ .



(c) Derive the expression for output voltage and draw the output voltage for this circuit with a sinusoidal input of 2.5 mV.



(d) Derive the expression for output voltage and draw the output voltage for this circuit with a sinusoidal input of 120 μV.



## SE - Sem-III - INST- (CBSGS) - Digital Electronics Nov- 15.

Q.P. Code: 5070

		(3 Hours)	[ Total Marks: 80
N.B.		<ol> <li>Question No.1 is compulsory.</li> <li>Attempt any three questions from the remaining.</li> <li>Assume suitable data if necessary.</li> </ol>	
i.	1	Answer the following (Any Four):  (a) Convert: (i) (77) <sub>8</sub> → (?) <sub>10</sub> (ii) (111010110000111) <sub>2</sub> → (?) <sub>16</sub> (b) Explain the working of SR Flip-flop. What is meant by edge to (a) Design half adder using logic gates	20 riggering?
		<ul> <li>(c) Design half adder using logic gates.</li> <li>(d) Explain the function of CMOS Inverter.</li> <li>(e) Determine the value of x, (193)<sub>x</sub> = (623)<sub>8</sub>.</li> </ul>	
2.	(a)	<ul> <li>(i) 96 - 78 using 2's complement.</li> <li>(ii) Add BCD 87 + 96.</li> <li>(iii) Subtract BCD 13 - 06.</li> <li>(iv) (1101)<sub>Binary</sub> → (?)<sub>gray</sub></li> <li>(v) (89A)<sub>16</sub> = (?)<sub>2</sub></li> </ul>	10
	(b)	Design 4 - bit binary to gray code converter.	10
3.	(a)	<ul> <li>Simplify using boolean laws and Implement using logic gates.</li> <li>(i) f = ABC + ABD + BD + BC</li> <li>(ii) f = AB + AC + BC</li> </ul>	10
	(b)	Simplify following using k-map and implement using logic gates $f = \sum (2,5,7,15) + d(6,9,13)$	. 10
4.	(a)	Design an adder to add two BCD numbers using four bit binary and necessary gates.	IC 7483 chips 10
		Convert D filpflop to T filpflop.	5
	(c)	Draw and explain the function of Ring counter.	5

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N.B.

5.	(a) (b)	Design MOD - 12 asynchronou Explain the operation of 4-bit bit	us ripple counter. idirectional shift register with neat diagran	10 m. 10
6.		te short note on (Any Four):		
	(a)	De Morgan's Theorem		20
	(b)	FPGA		
	(c)	DEMUX		
	(d)	ASCII Codes		

(e) ALU

(f) PAL and PLA.

## INST/Sem-III (CBSGS)/Transducers-I

Q.P. Code: 5165

			*	(3 Hours)	l Total Marks	3
N.B	. :	(1)	Question No.1 is	compulsory.		NET OF THE PERSON OF THE PERSO
		(2)		e from the remaining questions.		7,
		(3)		data wherever required and state	the assumptions	3
		(-)	1 10001110 0010010 0	wild will be a required with state		
1.	Ar	iswe	r in brief (any Four	r)	1138	20
		(8	a) Define transduc	cer and state their classification.	Lan	
			The second secon	g of Bimetallic thermometer.	OFT	
				gy and write its significance.	3	
		(0		ween direct and indirect methods	of level measurement	
		,	-	f each of these methods.	V	
		(6	e) Justify-LVDT	can be used as primary as well as	secondary transducer.	
2:	(a)	E	xplain the law of int	ermediate temperatures and law of	of intermediate metals	10
		in	case of thermocou	ple and give its significance.		
	b)	D	raw and explain any	y one method of humidity measu	irement.	10
					s same me o	
3.	a)			g resistance of 2500Ω is rated	_	
				excitation voltage? Calculate reso	-	
				iometer is 0, im and number of turn 67 at the travel, if meter is c		
			otentiometer.	or at the draver, it meter is co	onnected across the	
	(b)			f encoders. Explain with a neat sl	ketch any one of them	10
	(0)	Di	are different types o	Choose S. Daplan with a now si	toton any one or mont.	10
4.	(a)	E	xplain working princ	aple of capacitive transducer. Dray	w and explain different	10
			ethods to vary cap			
	(b)			stary displacement measurement	techniques.	10
5.	(a)	A	thermistor has a re-	sistance of 3980 $\Omega$ at the ice points	nt (0°C) and 794 Ω at	10
		5.0		temperature relationship is given b	by $R_T = a R_0 \exp(b/T)$ .	
			7 3	constants a and b		
				e range of resistance to be m	easured in case the	2
	-	4		varies from 40°C and 100°C.		3.2
	(b)	ZES.	xplain different typ	es of errors in measurements wi	th their remedies.	10
-	75	7	ala aut matati (Amii T	· · · · · ·		30
-	TIM	- 10	short notes: (Any T  1) Lead wire com	pensation in RTD.		20
1	-			E Level (SPL) meter		
-			3) Strain gauge			
			,			