/ SE/INST/ SEM III (CBSGS) T1723 / T1505 ELECTRICAL NETWORKS ANALYSIS & SYNTHESIS / MAY 2017

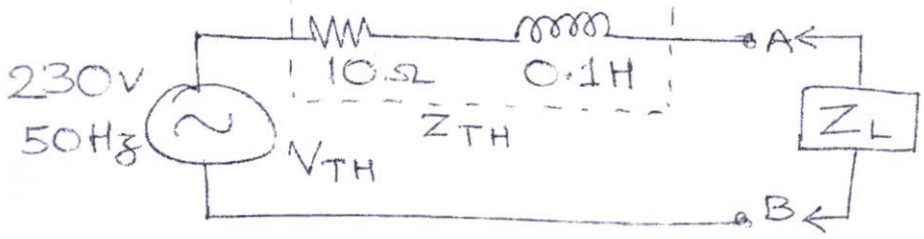
QP Code : 551002

(3 Hours) **[Total Marks : 80**

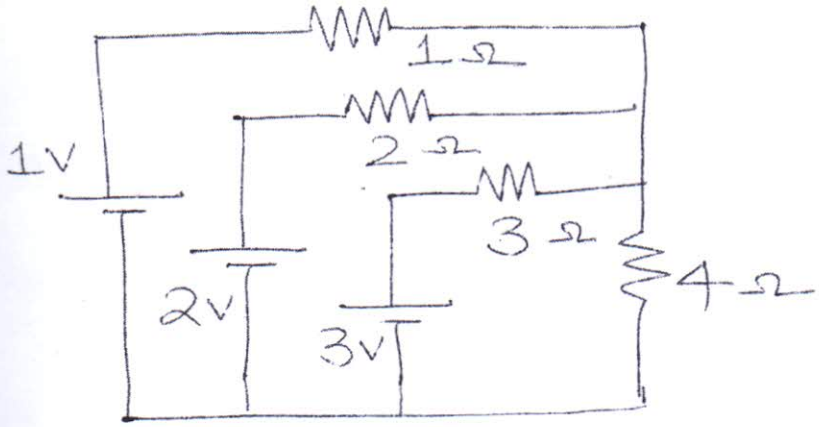
N.B. : (1) Question **No. 1** is Compulsory.
(2) Attempt **any three** questions from remaining **five** questions.
(3) **All** questions carry **equal** marks.

1. Attempt any **five** : **20**

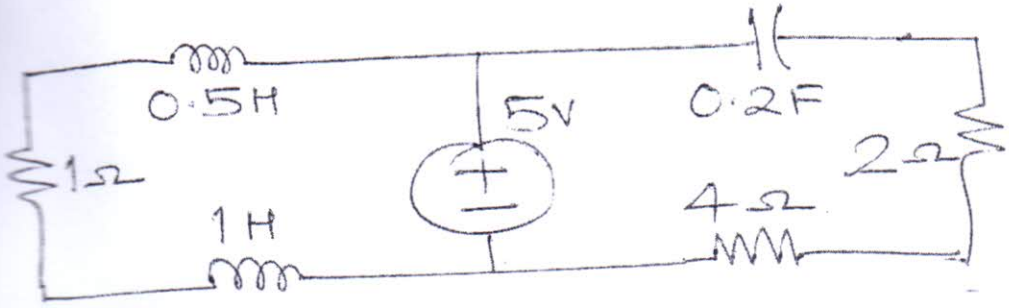
(a) Determine value of Z_L for maximum power transfer and calculate max. Power.



(b) Find $I_{4\Omega}$ using Nodal analysis.



(c) Obtain dual of given network



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(d) If $Z_{11} = 5\Omega$, $Z_{22} = 7\Omega$, $Z_{12} = Z_{21} = 3\Omega$ for a two part network, find ABCD parameters.

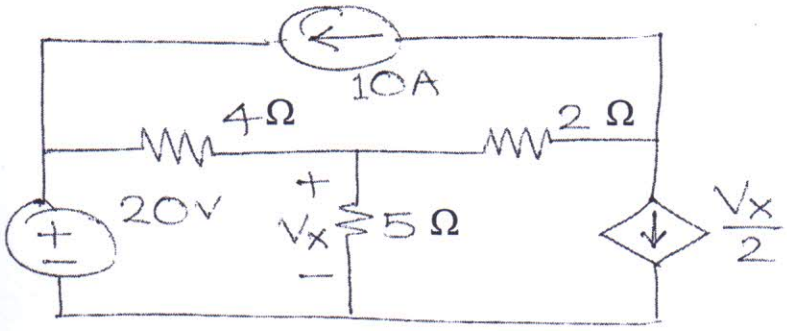
(e) Find the current through a capacitor of value 1/2 F given that voltage across capacitor is

$$V_C(s) = \frac{1}{S^2 + 1}$$

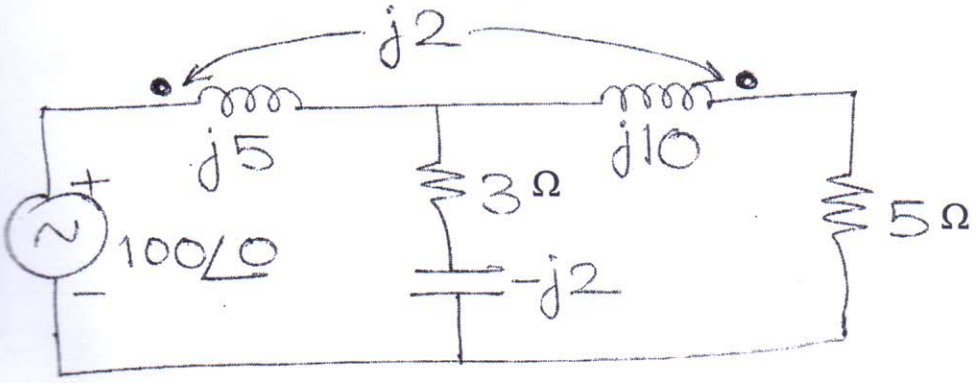
(f) Test whether following polynomial is hurwitz.

$$P(S) = S^5 + 2S^3 + S$$

2. (a) Find V_x using superposition theorm. **10**



2. (b) Find voltage across 5Ω resistor. **10**



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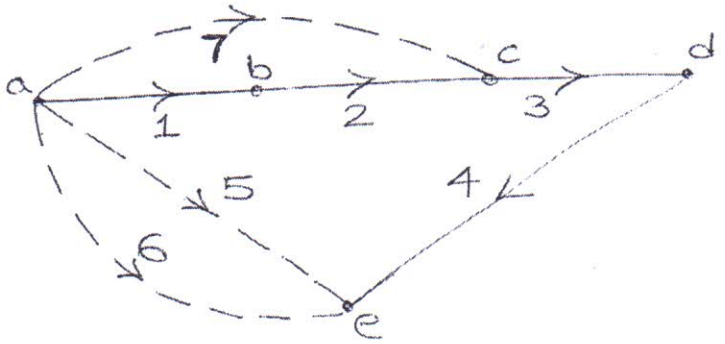
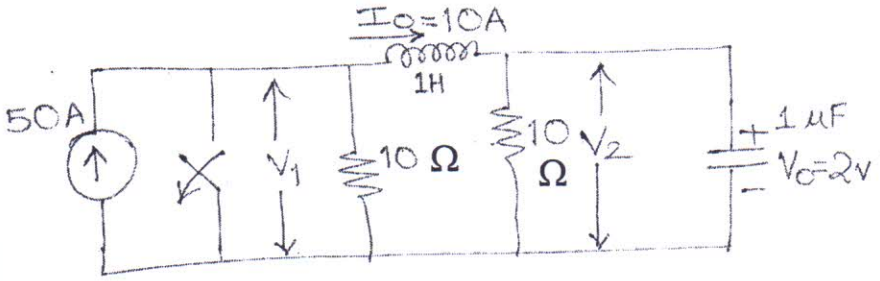
3. (a) For given tree, find **10**
   (i) Incidence Matrix (ii) f -cutset matrix

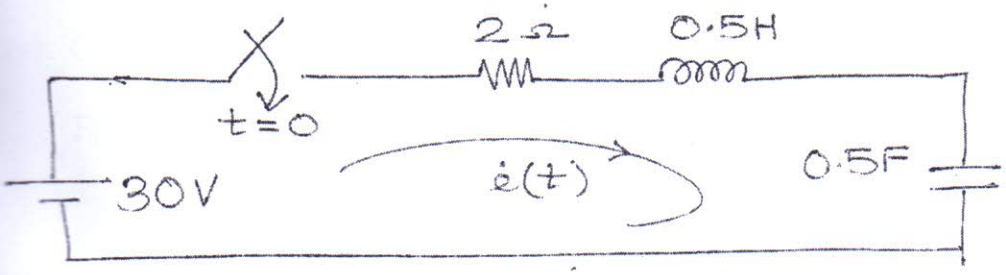


(b) For the network given below, switch is opened at t = 0 with initial conditions shown. Find the values of **10**

$$V_1, V_2, \frac{dv_1}{dt}, \frac{dv_2}{dt} \text{ at time } t = 0^+$$



4. (a) Obtain i (t) for the network shown. Use time domain approach. **10**



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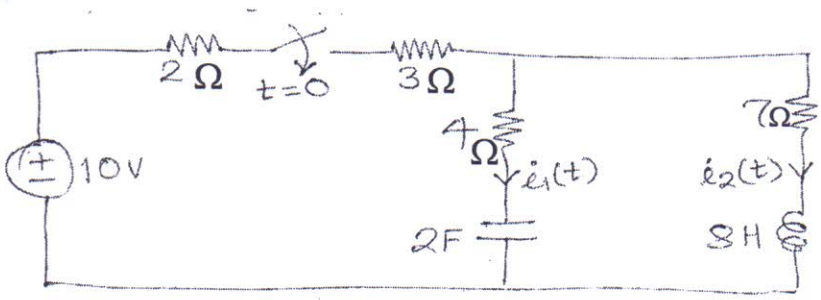
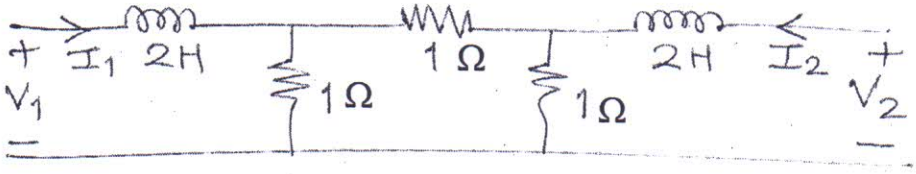
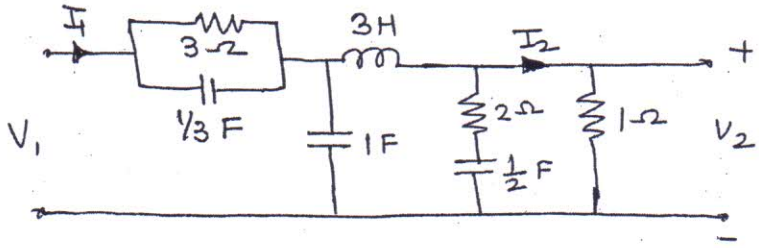
(b) Determine i_1 (t) and i_2 (t) **10**



5. (a) Find ABCD parameter **10**



(b) Determine $\frac{I_2}{I_1}$ for network



6. (a) Check for positive real function.

$$F(s)=\frac{2s^2+2s+1}{s^3+2s^2+s+2}$$ **10**

(b) $Y(S)=\frac{4(s^2+4)(s^2+25)}{s(s^2+16)}$ **10**

Find Foster II and Cauer I forms.

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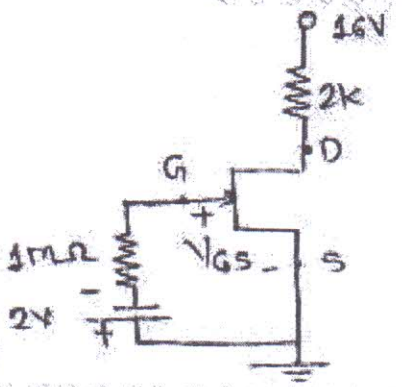
(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. 1 is **compulsory**.
(2) Attempt **any THREE** from remaining five questions.
(3) **All** questions carry equal maks.
(4) Assume suitable data wherever necessary.

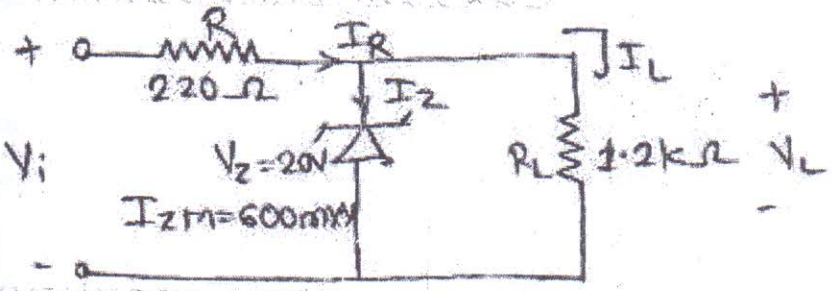
1. Anwer any four questions from the following :- **20**

a) Determine the following fo fixed bias configuation V_{GSQ}, I_{DQ}, V_{DS}, V_G, V_S.

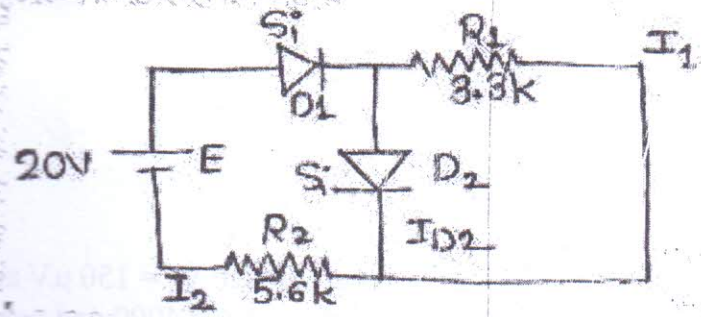


$I_{DSS} = 10mA$
$V_P = -8V$

b) Determine range of Vi that will maintain zener diode in ON state.



c) Determine I_1, I_2 and I_{D2} for network given below.



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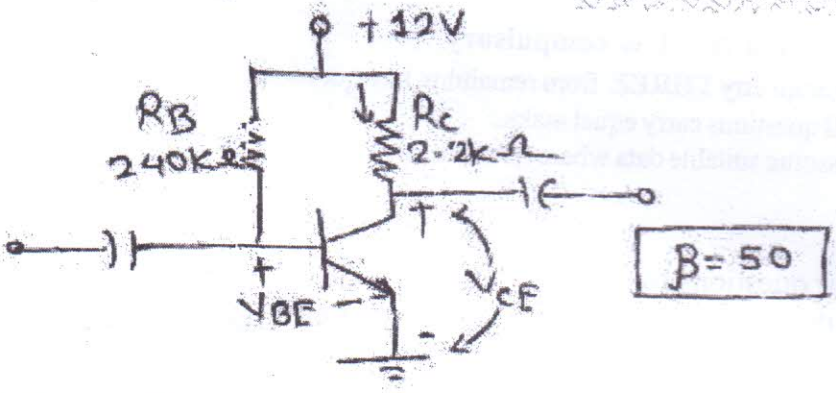
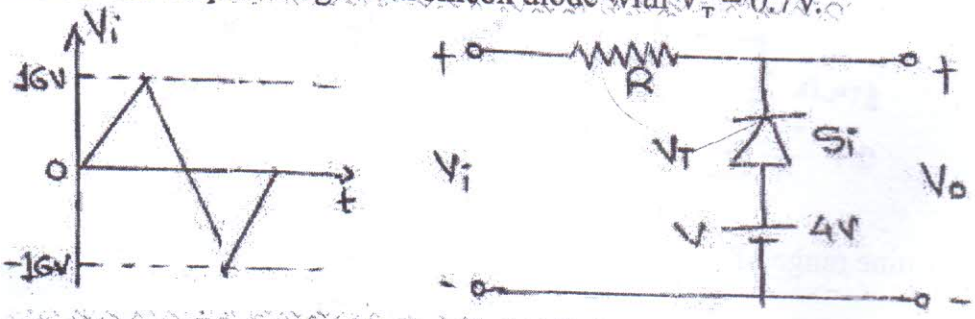
d) Find I_{CQ} and V_{CEQ} for given network.



e) Define rectifier and explain any one type of full wave rectification.

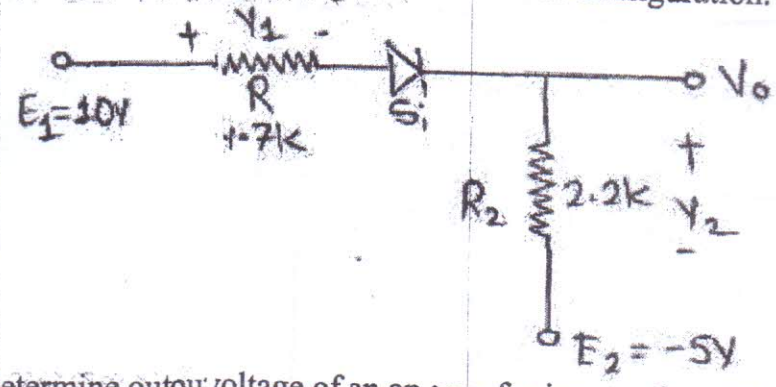
2. a) Determine output voltage with silicon diode with $V_T = 0.7V$. 8



b) Explain four types of controlled sources of op amp. 8

c) Op amp having SR = 2v/μS. What is maximum close loop gain that can be use when input signal varies by 0.5V in 10 μS. 4

3. a) Determine I_1, V_1, V_2 and V_0 for the series dc configuration. 5



b) Determine output voltage of an op amp for input voltage $V_{i1} = 150\ \mu V$ and $V_{i2} = 140\ \mu V$. The amplifier has a differential gain of Ad = 4000 and value of CMRR is 10(5

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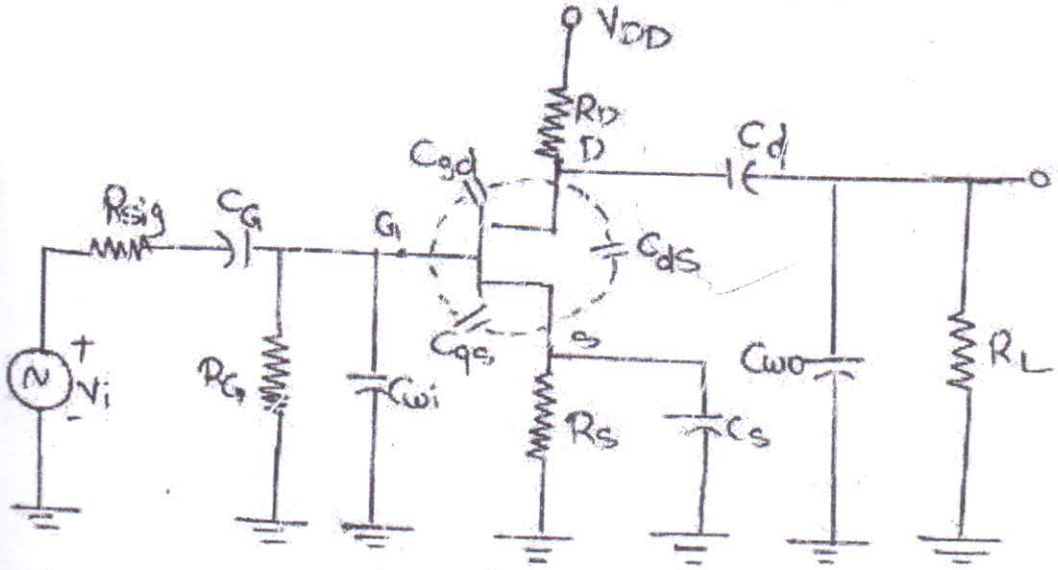
c) List the biasing techniques of FET And explain any two techniques in detail. **10**

4. a) Explain integrator and its frequency response. Explain how practical integrator overcomes disadvantages of basic integator. **10**

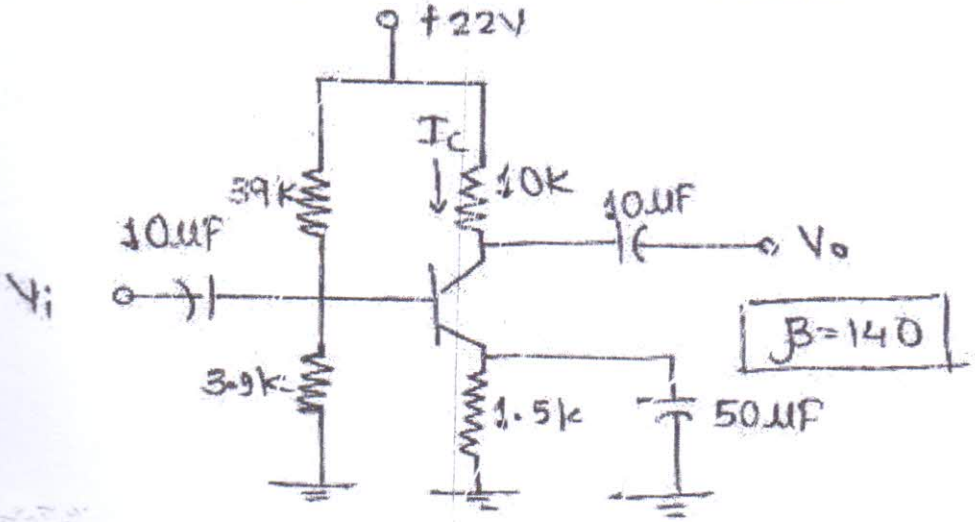
b) Define oscillator. State condition of oscillation. Explain RC phase oscillator. **10**

5. a) Determine high frequency and low fequency response of network shown Below **10**

C_G= 0.01 μF , C_C=0.5 μF , C_S=2 μF, Rsig=10KΩ, R_G=1MΩ
R_D=4.7KΩ , R_S= 1KΩ , R_L=2.2KΩ , I_{DSS}=8, V_P= -4V, rd=∞Ω , V_{DD}=20V
A_V = -3 , C_{gd}= 2pF , C_{gs}=4pF , C_{ds}=0.5pF ,C_{wi}=5pF , C_{wo}=6pF



b) Determine V_{CE} and current I_C fo voltage divider configuration. **10**



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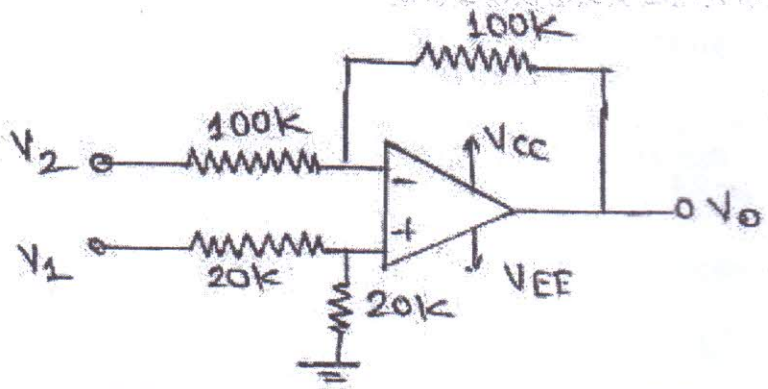
6. a) Draw and explain series voltage regulator. 5
   b) Write a note on Schmitt trigger. 5
   c) Bias compensation techniques. 5
   d) Derive expression for output voltage and hence determine output voltage when V1 = V2 = 1V. 5



SE | Inst | Sem III | CCBSCS) | Digital Electronics
May-17.

Q. P. Code : 550602

(3 Hours) **(Total Marks : 80)**

N.B. (1) Question no 1 is compulsory.
(2) Attempt any three questions from the remaining questions
(3) Figures to the right indicate full marks.
(3) Assume suitable data wherever necessary.

1. Answer the following (**any four**) **20**
(a) Convert: (i) $(24.165)_{10}$ into Hexadecimal, binary & octal number.
(b) Realize AND & EX-OR gate using NOR gate.
(c) Convert the following equation in standard SOP form.
$$Y = \overline{A}B + AC + BC$$
(d) Perform following operations.
(i) $(110011)_2$ - $(101100)_2$
(ii) $(101100)_2$ - $(110011)_2$
(e) Convert the binary number $(11011011.1102)_2$ into decimal, Hexadecimal & octal form.

2. (a) Design 32:1 Multiplexer using 8:1 Multiplexer & suitable gates. **10**
(b) Obtain the minimal expression using Quine Mc Cluskey method. **10**
f(A,B,C,D) = Sm(1,4,5,12,13,14)+d(2,7)

3. (a) Implement the following logic using 4:16 decoder. **10**
$F_1 = \Sigma m\ (1,2,4,8,11,12,13)$
$F_2 = \Sigma m\ (10,12,8,13,14)$
$F_3 = \Sigma m\ (2,3,4,11)$
$F_4 = \Sigma m\ (2,4,6,8)$
(b) Design mode 7 synchronous counter using J.K. flip flop. **10**

4. (a) Design 4 bit BCD adder using IC 7483. **10**
(b) Design & implement 4 bit binary to gray converter. **10**

5. (a) Explain the operating of 4 bit bidirectional shift register with neat diagram. **10**
(b) Draw & explain master slave JK flip flop. Describe how it eliminates race around condition. **10**

6. Write a short notes on:- (any four) **20**
(1) Explain CMOS inverter.
(2) Compare PAL & PLA.
(3) Compare T & D Flip Flop.
(4) Explain Johnson counter.
(5) State & prove De Morgan's theorem

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Q.P. Code : 550800

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No.1 is compulsory.
(2) **Attempt** any **three** out of remaining.
(3) Figures indicate to the **full** marks.
(4) Assume suitable data if necessary.

1. Answer the following. **20**
   a) Classify transducers with suitable example.
   b) Draw and explain Flapper-Nozzle system.
   c) What is the principle of working of capacitive transducers? How can we use them for level measurement?
   d) Find seebeck voltage for a thermocouple with proportionality constant of 40μV/°C If the junction temperature are 40°C and 80°C.
   e) A thermistor has a resistance temperature coefficient of -5% over a temperature range of 25°C to 50°C. If the resistance of the thermistor is 100 ohms at 25°C, what is the resistance at 35°C?

2. a) Draw and explain working of LVDT. What causes residual voltage to occur? **10**
   b) A linear resistance potentiometer is 50mm long and is uniformly wound with a wire having resistance of 10,000 Ω under normal condition. The slider is at the center of the pot. Find the linear displacement when the resistance of pot is measured by Wheatstone's bridge for two cases (i) 3850 Ω (ii) 7560 Ω. Are the two displacements in the same direction? **10**

3. a) Explain any five static characteristics of transducer with suitable examples. **10**
   b) What is the need of lead wire compensation? How it is to be done in RTD? What is self heating effect in RTD? **10**

4. a) For a certain thermistor β = 3140 K and at 27°C is known to be 1050 Ω. The thermistor is used for temperature measurement and the resistance measured is as 2330 Ω. Find the measured temperature. **10**
   b) Draw set up and explain working of air purge method of level measurement. **10**

5. a) Explain in detail radioactive type level detector. **10**

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b) A capacitive transducer uses two quartz diaphragm of area 750 mm^2 separated by a distance of 3.5 mm. A pressure of 900 KN/m^2 when applied to top diaphragm produces a deflection of 0.6 mm. The capacitance is 370pF when no pressure is applied to the diaphragm. Find the value of capacitance after the application of pressure 900 KN/m^2. **10**

6. Write short notes **(any two)** :- **20**

a) Optical pyrometer

b) Rotary encoder

c) Metrology & need of inspection
