TE / SEM-VI / CBSGS / ETRX / Nov 17

Basic VLSI Design

Q.P. Code :10652

[Time: 3 Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. Question No. 1 is **compulsory.**
2. **Attempt any three questions from remaining five questions.**
3. **Assume suitable data where required.**
4. **Figures** to the **right** indicate **full marks.**

Q.1 **(Solve any 4)**

a] Compare BJT & CMOS technology in VLSI design. **05**

b] Implement the following function using Static CMOS. **05**

$$Y = \overline{(A + B)(C + D)}$$

c] Implement half adder circuit using static CMOS. **05**

d] Implement 4*4. NAND based ROM array. **05**

e] Explain importance of Low power design. **05**

Q.2 a] What are the different MOSFET Models? Give importance of MOSFET capacitances related to MOSFET's performance. **10**

b] Explain transfer characteristics for CMOS Inverter showing different regions. What is the effect of variation in W/L ratio? **10**

Q.3 a] Draw 6T SRAM cell and explain it's read & write operation. **10**

b] Explain Scheme for multiplication of 110*100 **10**

Q.4 a] Explain various techniques of clock generation & clock distribution. **10**

b] Implement 4:1 multiplexer using NMOS pass transistor logic. **10**

Q.5 a] Draw D Flip Flop using CMOS and explain the working. **10**

b] Draw CLA (carry lookahead adder) carry chain using Static CMOS logic. **10**

Q.6 Write Short notes on. **20**

a] Interconnect Scaling

b] Latch up in CMOS

c] Decoder in Memory Structure.

d] ESD protection.

Q. P. Code: 25078

Time:-3 Hours **Marks:-80**

N.B (1) Question No. 1 is compulsory

(2) Attempt any 3 questions from remaining questions

(3) Figures to the right indicate full marks.

Q.1	a. Solve using Booth's algorithm Multiplicand M=+7 and Multiplier Q=+3.	5
	b. Write microinstructions for the instruction ADD R3, R2, R1.	5
	c. Explain SIMD computer organization.	5
	d. Explain various types of memories	5
Q.2	a. What is cache coherency? Explain various methods to achieve it.	10
	b. Explain various pipelining hazards and solutions for the same.	10
Q.3	a. Explain micro-programmed control unit with a neat diagram.	10
	b. Explain briefly various cache mapping techniques	10
Q.4	a .What is virtual memory? Explain how paging is implemented in virtual memory.	10
	b. Find page fault for the following string using FIFO, LRU and LFU page Replacement policies for the page address stream 2 1 2 3 1 5 4 2 1 5. Consider page frame size n=3.	10
Q.5	a. Explain various DMA transfer modes.	10
	b. Explain Flynn's classification.	10
Q.6	a. Explain various bus arbitration techniques.	10
	b. Explain the register structure of IA-32 family.	10

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Q. P. Code : 13681

REVISED COURSE

(3 Hours) **Total Marks: 80**

N.B. 1) Question No. 1 is compulsory.
2) Attempt any three questions out of the remaining five questions.
3) Figures to the right indicate full marks.
4) Assume suitable data wherever required but justify the same.

Q1 Answer **any four** 20

a) Compare the various triggering methods of thyristors.

b) What is the need of freewheeling diode in rectifiers? Explain with an example.

c) Draw and explain VI characteristic of TRIAC.

d) Explain the commutation techniques for SCR. Draw any one, forced commutation circuit.

e) Explain various control strategies for DC-DC converter.

Q2 a) Draw and explain single phase fully controlled converter with RL load .Draw load current, load voltage input voltage and gating signal for $\alpha = 60^0$. 10

b) Explain the working of three phase bridge inverter in 180 degree conduction mode with circuit diagram and waveforms. 10

Q3 a) A single phase full bridge inverter has a resistive load of 10 Ω and dc input voltage of 48 V. 10

Calculate : i) RMS output voltage V_{rms}

ii) RMS output voltage at fundamental frequency $V(01)_{rms}$

iii) Total Harmonic Distortion (THD)

iv) Average and peak current of each thyristor

b) Explain working principle of single phase cyclo converter with circuit diagram and waveforms. 10

Q4. a) A single phase fully controlled converter is operated from 230V, 50Hz ac supply. The load resistance is 10 Ohms. The average output voltage is 10% of max possible average output voltage. 10

Calculate:- i) Firing angle

ii) RMS and Average output current

iii) Efficiency

iv) Displacement Factor (DF)

b) Draw and explain the working of 3Φ fully controlled rectifier with neat circuit diagram and Waveforms. 10

Q5. a) Draw and explain AC voltage control circuit using DIAC and TRIAC .Draw the waveforms with- $\alpha = 45^0$. 10

b) Draw and explain Boost converter with waveforms. Also derive the expression for output voltage. 10

Q6. Write short notes on (**Any three**) 20

a) Compare IGBT, MOSFET and GTO.
b) Protection circuits for SCR.
c) Driver circuits for power transistors.
d) Voltage control of inverters using PWM techniques.

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ectronics/Sem:VI-(CBSGS)/Digital Signal Processing and Processors/Dec-2017

Q.P.Code: 016379

(3 Hours) **[Total Marks: 80]**

NB:

1) Question No. ONE is compulsory.
2) Out of remaining questions, attempt any THREE questions.
3) In all FOUR questions to be attempted.
4) All questions carry equal marks.
5) Answer to each new question to be started on a fresh page.
6) Figures in brackets on the right hand side indicate full marks.
7) Assume Suitable data if necessary

Q1. Attempt any four (20 marks)

a) Differentiate between Butterworth and Chebyshev filters.
b) Explain frequency wrapping effect in designing IIR filter.
c) State the relationship between DFS, DFT and Z transform.
d) What is DTFS. Find DTFS of x(n)={0,1,2,3) with period N=4.
e) Compare DSP processor and microprocessor.

Q2. a) Compute IDFT of the following sequence using inverse FFT algorithm X(k) = {3,0,3,0,3,0,3,0} (10 marks)

b) Write down design steps for FIR filter using window techniques. Compare windows. (10 marks)

Q3. a) Design analog Butterworth filter that has -2 dB passband attenuation of 20 rad/sec and at least -10 dB stopband attenuation at 30 rad/sec. (10 marks)

b) Compute the circular convolution of the sequence using DFT and IDFT, x1(n)={1,2,0} and x2(n)={2,2,1,1) (10 marks)

Q4. a) Given H(s)= [1/ (s+1)(s+3)], T=2 seconds. Design digital IIR filter using BLT method. Explain advantages of BLT over IIM method. (10 marks)

b) Design 6th order linear phase LPF with cut off frequency $\pi/2$ using Blackman window. (10 marks)

Q5. a) Design Butterworth LPF to meet following specifications

Passband gain is 0.89
Passband frequency edge 30Hz
Attenuation 0.20
Stopband edge 75Hz (10 marks)

b) Design the symmetric FIR LPF where desired frequency response is given as

$$Hd(w)=\begin{cases} e^{(-jwt)} & \text{for } |w|\leq w_c \text{ otherwise} \\ 0 \end{cases}$$ (10 marks)

Q6. Write short note on following (Any two) (20 marks)

a) Gibb's Phenomenon
b) Application of DSP in speech and Radar processing
c) Limit cycle Oscillations