ETRX / Paper / Subject Code: 37201 / BASIC VLSI DESIGN

TE / Sem- VI - CBSGS / NOV-2018.

**Duration:3 hrs** **Maximum Marks :80**

**Note:** 1.Question 1 is compulsory.

2.Solve any three out of remaining .

3.Assume suitable data if necessary

4.Draw proper diagrams

**Q.1. Solve any four.**

(a) Compare Biploar,NMOS and CMOS technologies (min three points) . [5]

(b) Design a 2:1 MUX using transmission gates and discuss advantages of use of transmission gate logic. [5]

(c) Implement $Y=\overline{(A.B)+(C.D)}$ using Dynamic Logic. [5]

(d) Compare Ram and ROM. [5]

(e) Explain clock generation techniques. [5]

**Q.2 (a)** Sketch and explain the general shape of the Transfer characteristics of NMOS inverter.Compare different types of inverters. [10]

(b) Compare the full scaling model with constant voltage scaling model for MOSFETS. Demonstrate clearly the effects of scaling on the device density, speed of the circuit, power consumption and current density of the gates [10]

**Q.3 (a)** Implement D flip-flop using Static CMOS. What are other design methods for it? [10]

**(b)** Explain READ and WRITE operation of 6-T SRAM cell in detail. [10]

**Q.4 (a)**What is ESD protection? Explain with example. [10]

**(b)** Explain Carry Look Ahead adder and it's advantages. [10]

**Q.5 (a)**What are different clock distribution schemes? Explain concept of Global and Local clock. [10]

**(b)** What are various decoders used in memory structures? Explain any one in detail. [10]

**Q.6.** Write short notes on (any three) [20]

(a) NORA ,Zipper Logic design (b) Flash Memory

(c) CMOS latch-up and its prevention.(d) Sense Amplifier

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Electronics / SEM VII (CBSGS) / NOV. 2018

Paper / Subject Code: 37202 / ADVANCED INSTRUMENTATION SYSTEM

**Q. P. Code: 22742**

**Total Marks: 80** **Time: 3 Hours**

Note: 1) Question No.1 is compulsory.

2) Attempt any three questions from remaining five questions.

3) Assume suitable data if necessary.

4) Figures to the right indicate full marks.

Q.1 Explain in brief

a) Data logger 5M

b) Derivative controller 5M

c) Sequence valve 5M

d) Smart transmitter 5M

Q.2) a) What is the necessity of the positioner. Draw the diagram for any one valve positioner and give the details. 10M

b) Explain the control valve characteristics with diagram. A velocity control system has a range of 200 to 480 mm/s. If the set point is 327 mm/s and the measured value is 294 mm/s, calculate the error as % of span. 10M

Q.3) a) Give the comparison details of electrical, pneumatic and hydraulic systems. 10M

b) Explain methods for local pressure control with diagram. 10M

Q.4) a) Give the classification of compressors. Explain any two rotary compressors with diagram. 10M

b) What is Transmitter? Give the classification details of transmitters. Draw and Explain a process loop with transmitter. 10M

Q.5) a) Explain flapper nozzle system. Explain any two applications of flapper nozzle system for industrial use. 10M

b) What is the necessity of controller tuning? Explain any two methods of controller tuning? 10M

Q.6) a) With neat block diagram, explain the working of multichannel data acquisition system. 10M

b) Write short note on 10M

i) Actuator selection parameters

ii) Double acting cylinder

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ETRX / Paper / Subject Code: 37203 / COMPUTER ORGANIZATION / Nov-2018

Sem- VI - CBSGS.

Q.P. Code: 36598

Duration: 3 Hours

Marks: 80

N.B: (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1(a) Consider the following code

```
for(m=10;m>0;m--)
{
a[m]=a[m]+2
}
x=y+2;
x=x%2;
```

State the spatial locality and Temporal Locality in the code. 4

(b) State the advantages of Vertical Microinstructions over Horizontal Microinstructions. 4

(c) Consider the execution of a Program with 15000 instructions by a linear pipeline processor with a clock rate of 25 Mhz, Assume that the instruction pipeline is 5 stages one instruction is issued per clock cycle. The penalties due to branch instructions are ignored .

i) Calculate the speedup factor as compared with Non Pipelined processor.

ii) What is efficiency and throughput of this pipelined processor? 4

(d) Compare the RISC and CISC features 4

(e) Differentiate between Cache Look Aside Architecture and Cache Look through Architecture. 4

Q2 (a) Explain the Write Techniques in Cache Memory .Explain how Snoopy Controller Is used to implement Cache Coherency. 10

(b) Consider a 4-way set associative Cache Mapping with Cache Block Size=16 bytes Cache size=8k, Main Memory Size =64k. Design a cache structure and show how the Processor address is interpreted. 10



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Q3 (a) Explain the Virtual Address to Physical address Translation for the following specifications Virtual Memory=128k and Main Memory=32k, page size = 1k .Illustrate Page Fault with the help of a example. 12

(b) Compare Paging and Segmentation 8

Q4 (a) Explain the various I/O Data transfer Techniques. 8

(b) Explain Microprogrammed Control Unit and compare its Control Memory with Nano-Programming. 12

Q5 (a) Explain the different addressing modes of IA-32 with suitable examples. 8

(b) Write microinstructions for the instruction MOV [ $R_0$ ], $R_3$ . Explain the Hardwired control unit with reference to the above instruction. Design a Combinational circuit to generate the RUN control signal using suitable control signals. 12

Q6) Write short notes on

a) Memory Interleaving 6

b) Flynn's Classification 7

c) Page Replacement policies 7



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**Q. P. Code: 21941**

**Time: 3 Hours** **Marks: 80**

**Instruction to the candidate if any :-**

**N.B.**

1) **Question No-1 is Compulsory.**
2) **Attempt any Three (03) Questions from remaining Five (05) Questions.**
3) **Assume suitable data where ever necessary.**

| Q. No. | | Marks. |
|---|---|---|
| Q.1 | **Attempt the following Questions(any4)** | |
| | a) Equivalent circuit and circuit symbol of IGBT | 5 |
| | b) Compare Self commutation and Class D Commutation . | 5 |
| | c) What is difference between a cycloconverter and an ac voltage controller | 5 |
| | d) What are the performance parameters of Inverter ,give effect of crass conduction | 5 |
| | e) Explain brief step Down /Buck switching Regulator | 5 |
| | f) Calculate output voltage for a step up chopper with Vin= 200v and duty cycle= 0.25. | 5 |
| Q.2(a) | What are the over current protection SCR? State the crossbar protection circuit of SCR, Explain the metal oxide Varistors | 10 |
| Q.2(b) | What is difference between a cycloconverter and an ac voltage controller, Explain single phase converters with waveforms | 10 |
| Q.3(a) | Explain the construction of GTO I-V characteristics of GTO with Advantages of GTO over BJT and SCR & Applications of GTO | 10 |
| Q.3(b) | Draw and Explain Buck-Boost Converter with the help of circuit diagram and waveforms Derive the relation for load voltage | 10 |
| Q.4(a) | A SINGLE quadrant DC to DC converter is operated with following specifications 1.ideal battery of 220V 2.ON time $t_{ON}$ =2msec.3.OFF time $t_{OFF}$=1.5msec. To find 1.Average and RMS out put Voltage 2.RippleFactor and Form Factor | 10 |
| Q.4(b) | Draw and Explain Structure of power MOSFET? State STATIC &SWITCHING Characteristics, power MOSFET with forward blocking and applications of power MOSFET | 10 |
| Q.5(a) | Draw and Explain single phase half controlled rectifier with symmetrical configuration with highly inductive Load draw the waveforms | 10 |
| Q.5(b) | A three phase inverter operated in $180^0$conduction mode is operating from 470VDC supply find out the following 1.RMS value of output line and phase voltage 2.RMS value of the fundamental components of line and phase voltages | 10 |
| Q.6 | Write short note on:<br>(a) Full wave controlled rectifiers with R load with waveforms<br>(b) Three phase full wave converter with waveforms<br>(c) Dual Converter<br>(d) Construction& operation of IGBT | 20 |

Paper / Subject Code: 37205 / DIGITAL SIGNAL PROCESSING AND PROCESSORS /NOV.18

SEM VI (CBSGS)

Q. P. Code: 27628

Time: 3 Hours

Marks: 80

N.B.: 1. Question No. 1 is compulsory.
2. Attempt any three questions out of remaining five questions.
3. Figures to the right indicate full marks.
4. Assume suitable data if required and mention it in answer sheet.

Q1. (20 Marks)

a) Compare DSP and Microprocessor
b) Explain quantization effect in computations of DFT
c) Explain subband coding.
d) Explain limit cycle oscillations.

Q2. a) Write design steps of FIR filter using window techniques. Compare windows. (10 Marks)

b) Explain VLIW architecture in details. (10 Marks)

Q3. a) Explain Gibbs phenomenon in details (10 Marks)

b) Explain different addressing modes of TMS320C67XX DSP processor (10 Marks)

Q4. a) Design a linear phase FIR highpass filter using hamming window, with a cutoff frequency, $w_c = 0.8\pi$ rad/sample and N = 7 (10 Marks)

b) Explain in details application of Digital Signal Processor in Biomedical and Audio. (10 Marks)

Q5. a) Find the DFT of the following sequence using DIT-FFT ,x[n] = {1, 1, 1, 1, 1, 1, 0, 0 } (10 Marks)

b) Justify many to one mapping in s-plane to z-plane in Impulse Invariance method. Compare it with the mapping in Bilinear transformation. (10 Marks)

Q6. a) Compare IIR and FIR filters. (20 Marks)
b) Prove Parseval's theorem for the sequence x[n]={1,2,1, 0}
c) Explain frequency wrapping in IIR filter
d) Explain Silent features of TMS320C67XX DSP processor

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