TE/ETRX/Sem-VI/C2019/Basic VLSI Design

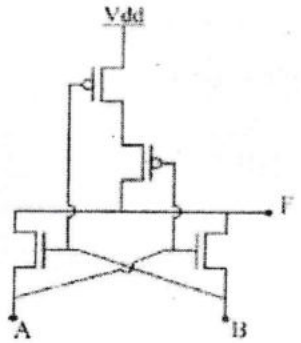
University of Mumbai

Examinations Summer 2022

Paper Code: 92057

Time: 2 hour 30 minutes

Max. Marks: 80

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1	Which condition is true for scaling factor S:
Option A:	S<1
Option B:	S=1
Option C:	S=0
Option D:	S>1
2	If the Noise Margin of the circuit increases then Noise Immunity
Option A:	Increases
Option B:	Decreases
Option C:	No change
Option D:	All of the above
3	How many MOS require for designing 2-i/p NAND Gate using static CMOS Design Style.
Option A:	NMOS-1, PMOS-2
Option B:	NMOS-2, PMOS-2
Option C:	NMOS-1, PMOS-1
Option D:	NMOS-2, PMOS-1
4	For a symmetric CMOS inverter, which condition is true?
Option A:	$(W/L)_P = 1.5\ (W/L)_N$
Option B:	$(W/L)_N = 1.5\ (W/L)_P$
Option C:	$(W/L)_P = 2.5\ (W/L)_N$
Option D:	$(W/L)_N = 2.5\ (W/L)_P$
5.	CMOS domino logic is the same as _____ with an inverter at the output line.
Option A:	clocked CMOS logic
Option B:	dynamic CMOS logic
Option C:	gate logic
Option D:	switch logic
6	In the circuit shown, A and B are the inputs and F is the output. What is the functionality of the circuit? 
Option A:	XOR
Option B:	SRAM Cell
Option C:	Latch

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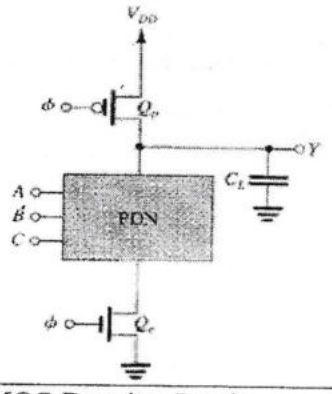
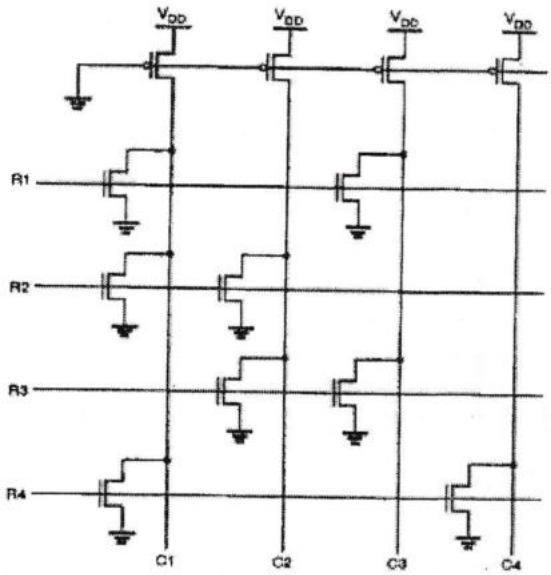
Option D:	NOR
7	Following diagram represents which design style : 
Option A:	CMOS Domino Logic
Option B:	CMOS static logic
Option C:	Pass transistor logic
Option D:	CMOS Dynamic Logic
8	In the following circuit if R1, R2, R3, R4 logic level is 0001 then C1,C2,C3,C4 logic level will be 
Option A:	0101
Option B:	0011
Option C:	0110
Option D:	1001
9	All DRAM requires periodic refreshing of data because
Option A:	Stored data can be modified
Option B:	Data stored as charge in a capacitor can't be retain indefinitely
Option C:	Stored data can be erased
Option D:	Data can be written in memory

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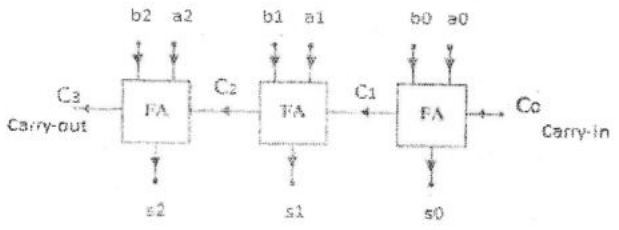
10.	 Adder circuit shown in the above fig. is..... where a_n and b_n are input bits and C_n & S_n arecarry and sum respectively.
Option A:	3bit Carry look ahead adder
Option B:	4 bit Carry look ahead adder
Option C:	3 bit Ripple Carry Adder
Option D:	4 bit Ripple Carry Adder

Q2	**Solve any Four out of Six** **5 marks each**
A	Compare Bipolar, NMOS and CMOS technologies.
B	Compare SRAM and DRAM.
C	Design a 4:1 MUX using nMOS pass transistor logic.
D	Draw VTC of CMOS inverter. Show all critical voltages in it.
E	Compare Static CMOS, Dynamic CMOS and Pseudo nMOS logic.
F	Explain basic Manchester Carry Circuit with suitable diagram.

Q3	**Solve any Two Questions out of Three** **10 marks each**
A	Calculate noise margin of a CMOS inverter with the given parameters: NMOS $V_{To,n}$=0.6V , k_n=200uA/V^2, PMOS $V_{To,p}$=-0.7V , k_p=80uA/V^2, V_{DD}= 3.3V.
B	Implement the following function $Y=\overline{(A+B)(C+D)E}$ using: I) Static CMOS Logic II) Dynamic CMOS Logic III) Pseudo nMOS Logic
C	Draw 6T SRAM cell structure using MOS. Explain read, write and hold operations in detail.

Q4	
A	**Solve any Two** **5 marks each**
i.	Design a 4*4 NAND based ROM, which stores the following words: Row(0) 1000 Row(1) 1111 Row(2) 0111 Row(3) 1110
ii.	Design a half adder using Transmission Gate logic.
iii.	Compare Constant Voltage scaling and Full scaling with respect to following MOS parameters: Oxide Capacitance, Packing Density, Power Dissipation, Drain current and Saturation Current.
B	**Solve any One** **10 marks each**
i.	Explain 4 bit CLA adder with its carry equation. Draw the logical network using dynamic CMOS logic.
ii.	Design Master slave JK Flip Flop using any MOS Design Style.

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University of Mumbai
Examination 2022 under Cluster
(Lead College:)

Paper Code: 93463

Examinations Commencing from 17th May 2022

Program: **Electronics Engineering**

Curriculum Scheme: Rev-2019

Examination: **T.E. Semester VI**

Course Code: **ELC602** Course Name: **Electromagnetic Engineering**

Time: 2:30-hour Max. Marks: 80

N.B. Use Smith Chart to solve transmission line Problem

Q1	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks (20 Marks)**
1.	Find the force in N between Q1 = 2C and Q2 = -1C separated by a distance 1m in air.
Option A:	18×10^{6} N
Option B:	-18×10^{6} N
Option C:	18×10^{-6} N
Option D:	-18×10^{-6} N
2.	Gauss's law is true only if force due to a charge varies as
Option A:	r^{-1}
Option B:	r^{-3}
Option C:	r^{-2}
Option D:	r^{-4}
3.	Find the displacement current when the flux density is given by t^3 at 2 seconds
Option A:	12
Option B:	6
Option C:	3
Option D:	27
4.	The magnetic vector potential for a line current will be inversely proportional to
Option A:	dl
Option B:	I
Option C:	J
Option D:	R
5.	Displacement current depends on
Option A:	Moving Charges
Option B:	Change in time
Option C:	Moving Charges and Change in time
Option D:	Differential Moving Charges and cumulative time period
6.	The inductance of single-phase, two-wire transmission line per kilometer gets doubled when the
Option A:	Distance between the wires is increased as square of original distance

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Paper Code: 93463

Option B:	Distance between the wires is doubled
Option C:	Distance between the wires is increased four fold
Option D:	Radius of the wire is doubled
7.	The characteristic impedance of a transmission line with impedance and admittance of 16 Ω and 9 ℧ respectively is
Option A:	0.75
Option B:	1.33
Option C:	7
Option D:	25
8.	The ratio of radiation intensity in a given direction from antenna to the radiation intensity over all directions is called as
Option A:	Gain of antenna
Option B:	Radiation power density
Option C:	Array Factor
Option D:	Directivity
9.	In which of the following the power is radiated through a complete spherical surface
Option A:	Half-wave dipole
Option B:	Quarter-wave Monopole
Option C:	Both Half-wave dipole & Quarter-wave Monopole
Option D:	Full wave dipole
10.	The effects of EMI can be reduced by
Option A:	Suppressing emissions
Option B:	Reducing the efficiency of the coupling path
Option C:	Suppressing emissions, Reducing the efficiency of the coupling path and Reducing the susceptibility of the receptor
Option D:	Increasing the efficiency of the coupling path and emissions

$u = 0.6c$

Q2.	**Solve any Two of the Following** **20 Marks**
A	Derive an expression of Electric Field Intensity due to infinite line charge at any point P on z-axis.
B	A lossless transmission line with $Zo = 50\ \Omega$ is 30 m long and operates at 2 MHz. The line is terminated with a load $\boldsymbol{Z_L} = 60 + j40\ \Omega$. If u 5 $0.6c$ on the line, where c is velocity of light. Use Smith Chart to find (a) The reflection coefficient Γ (b) The standing wave ratio s (c) The input impedance Z_i
C	Write Maxwell's equations in time harmonic field form

Q3.	**Solve any Two of the Following** **20 Marks**
A	State and explain Maxwell's equations for differential and integral form for static field.
B	State Poynting theorem and derive an expression for the Poynting vector. Explain the power terms mentioned in the derivation

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Paper Code: 93463

C	Derive an expression for transmission line equation for two wire line problem.

Q4.	Solve any Two of the Following	20 Marks
A	Explain the terms radiation pattern, directivity, Beam-width and directive gain of the antenna.	
B	Explain in detail the sources and the characteristics of EMI. EMI control techniques.	
C	Write Short Notes on: (1) Horn Antenna (2) Microstrip Antenna	

212 – Pallavi Gaigule
213 – Himani Patel.
214 – Shobhit Khandare

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University of Mumbai

Examinations Summer 2022

Program: **Electronics Engineering** Paper Code - 93509

Curriculum Scheme: Rev2019

Examination: TE Semester VI

Course Code: ELC603 and Course Name: Computer Communication Networks

Time: 2 hour 30 minutes Max. Marks: 80

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Network topology in which you can connect each node to the network along a single piece of network cable is called
Option A:	Star topology
Option B:	Bus topology
Option C:	Mesh topology
Option D:	Ring topology
2.	Which OSI layer is known as Medium Access control Layer (MAC)
Option A:	Physical Layer
Option B:	Application Layer
Option C:	Transport Layer
Option D:	Data Link Layer
3.	Which of the following best suits the User Datagram Protocol (UDP)
Option A:	Unreliable
Option B:	Congestion Control
Option C:	Flow Control
Option D:	Velocity Control
4.	What is the size of the IP address of IPv4 in bytes?
Option A:	32
Option B:	16
Option C:	4
Option D:	10

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Paper Code 93509

5.	In the network layer which addressing is done?
Option A:	Physical addressing
Option B:	Logical addressing
Option C:	Port addressing
Option D:	Specific addressing
6.	Which of the following is used for short range communication?
Option A:	Fiber optic cable
Option B:	Infrared wave
Option C:	microwave
Option D:	Coaxial cable
7.	The transition from IPv4 to IPv6 is not possible from the following strategies
Option A:	Dual Stack
Option B:	Subnetting
Option C:	Tunneling
Option D:	Header translation
8.	In _____, the chance of collision can be reduced if a station senses the medium before trying to use it
Option A:	MA
Option B:	CSMA
Option C:	CDMA
Option D:	FDMA
9.	Data field is not present in following frame
Option A:	I-frame
Option B:	U-frame
Option C:	S-frame
Option D:	A-Frame

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Paper code 93509

10.	Simple Mail Transfer Protocol (SMTP) is_____
Option A:	Pull Protocol
Option B:	Push Protocol
Option C:	Forward Protocol
Option D:	Backward Protocol

Q2	**Solve any Two Questions out of Three** **10 marks each**
A	Describe different Addresses (MAC address, IP address, Port address, Specific address) used in networking with examples
B	Describe ADSL with respect to channel configuration, Modulation technique and Equipment setup
C	Explain Stop-And-Wait ARQ Protocol & list the advantages & disadvantages of Stop-And-Wait ARQ Protocol

Q3	**Solve any Two Questions out of Three** **10 marks each**
A	Draw and explain IPV4 header. Compare IPV4 with IPV6
B	Explain TCP/IP Protocol Suite. Distinguish between OSI model and TCP/IP model
C	Explain Sliding window flow control protocol with the help of suitable diagram

Q4	**Solve any Two Questions out of Three** **10 marks each**
A	What are causes & effects of Congestion in the Transport layer? Explain different congestion control mechanisms
B	Explain Time Slot Interchange Switch with the help of suitable diagram
C	Explain Domain Name System (DNS) in application layer with the help of suitable diagram

University of Mumbai
Examination Summer 2022

Program: BE Electronics Engineering

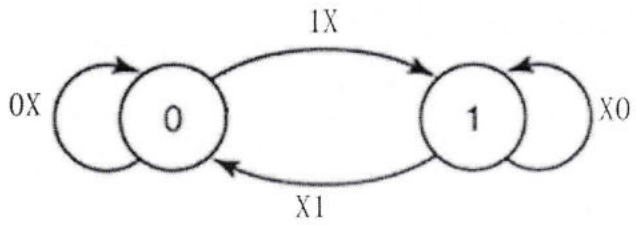
Program No.: 1T01136

Name of the Examination:T.E. (Electronics Engineering) (SEM-VI)

(Choice Base Credit Grading System) (R- 19) (C Scheme)

Subject (Paper Code) :89368 / / Digital Design with Reconfigurable Architecture (DLOC)

Time: 2-hour 30 min Paper code-94325. **Max. Marks: 80**

Note:- Choose the correct option for the following questions. All the questions are compulsory and carry equal marks.	
Q1.	If the declarative part in the architecture of a half adder is as below, identify the type of architecture. component XOR2 port (X,Y:in BIT, z: out BIT); end component; component AND2 port (L,M:in BIT, z:out BIT); end component;
Option A:	behavioral
Option B:	structural
Option C:	dataflow
Option D:	mixed Design
Q2.	Which flipflop does possess the following state diagram? 
Option A:	JK flip flop
Option B:	T flip flop
Option C:	SR flip flop
Option D:	D flip flop

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Paper code - 94325

Q3.	Which Method is not a State Reduction Technique?
Option A:	Implication Chart Method
Option B:	Inspection Method
Option C:	Partition Method
Option D:	One-Hot Encoding Method
Q4.	***process (clk)*** ***variable A,B,C,D: std_logic:= '0';*** ***begiin*** ***if clk'event and clk='1' then*** ***A <= Sin:*** ***B <= A;*** ***C <= B;*** ***D <= C;*** ***end if;*** ***Pout <= A&B&C&D;*** ***end process*** In the above code, if input signal Sin = '1' then at the end of 1 cycle at clk, the output Pout will be……..
Option A:	0001
Option B:	0000
Option C:	1000
Option D:	1111
Q5.	Which among the following state machine notations are generated outside the sequential state machine?
Option A:	Input variables
Option B:	Output variables
Option C:	State variables
Option D:	Excitation variables
Q6.	In VHDL an attribute, S ' LAST_EVENT returns …...
Option A:	Boolean value TRUE or FALSE
Option B:	Bit '1' or '0'
Option C:	Last value of S
Option D:	the time since the last event on signal S
Q7.	Which of the following is the correct sequence of steps of Digital design with FPGA?
Option A:	Design Entry, Mapping, Place and route, Simulation, Bit stream generation, Synthesize
Option B:	Design Entry, Simulation, Synthesize, Mapping, Place and route, Bit stream generation
Option C:	Bit stream generation, Design Entry, Simulation, Synthesize, Mapping, Place and route
Option D:	Simulation, Synthesize, Design Entry, Place and route, Mapping, Bit stream generation

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Paper code - 94325

Q8.	What does an arrow indicate in the schematic format of process statement given below? ?
	ma: Process (a,b,c,d_ in)
	Variable m_tmp:bit_vector(7 down to zero):="00000000",
	Begin
	div_tmp:= a/b;
	diff<=div_tmp- c-d_in;
	End process

Option A:	Variable declaration
Option B:	Process body
Option C:	Process label
Option D:	Sensitivity List
Q9.	Characteristic equation of J-K flipflop is……..
Option A:	$Q_{n+1} = Q'_nJ + Q_nK'$
Option B:	$Q_{n+1} = Q_nJ + Q'_nK'$
Option C:	$Q_{n+1} = Q_nJ' + Q_nK$
Option D:	$Q_{n+1} = Q'_nJ' + Q_nK$
Q10.	Which mode in VHDL allows to make the signal assignments to an output port while preventing it from reading?
Option A:	IN
Option B:	INOUT
Option C:	OUT
Option D:	BUFFER

Q.2	**Answer any Two questions out of Three (10 marks each)**
A	Write a VHDL code that divides the Clock frequency by 10.
B	i)Write a VHDL code of T flipflop. ii)Using T flipfop as a component write a code for 4 bit asynchronous counter.
C	Write a VHDL code for serial adder.

Q.3	**Solve any two questions out of Three (10 marks each)**
A	Write short notes on the following: i) Clock management in FPGA. ii) Operators used in VHDL with examples
B	i) Explain Booth Multiplication with example. ii)Write a VHDL code for Booth's multiplier.
C	Explain SRAM based FPGA architecture in detail.

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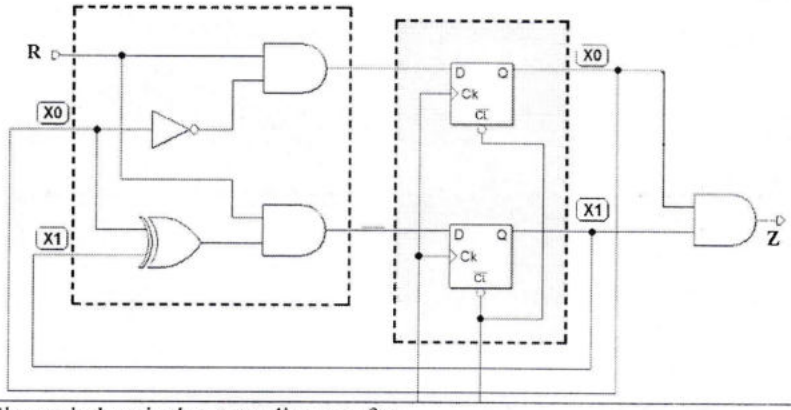
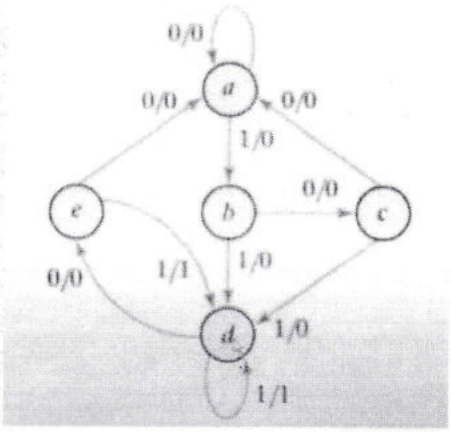
Paper code - 94325

Q.4	**Answer any Two questions out of Three** **(10 marks each)**
A	Design a Mealy sequence detector circuit to detect an overlapping sequence "10110" using D flip flop and logic gates.
B	Analyze the sequential-state machine shown in the following figure. Obtain state table and state diagram for the same. 
C	Shown below is the state diagram for sequential machine reduce it and design using D Flip Flop. 

TE / ETRX / Sem-VI / C2019 / Machine Learning / May-2022

University of Mumbai

Examinations Summer 2022

Time: 2 hour 30 minutes

Paper Code-93775

Max. Marks: 80

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Machine learning is a branch of..
Option A:	Artificial intelligence
Option B:	speech processing
Option C:	Language processing
Option D:	java
2.	What does K stand for in K mean algorithm?
Option A:	Number of Clusters
Option B:	Number of Data
Option C:	Number of Attributes
Option D:	Number of Iterations
3.	Feature selection tries to eliminate features that are
Option A:	Rich
Option B:	important
Option C:	Irrelevant
Option D:	Relevant
4.	During the treatement of cancer patients , the doctor needs to be very careful about which patients need to be given chemotherapy. Which metric should we use in order to decide the patients who should given chemotherapy?
Option A:	precision
Option B:	recall
Option C:	call
Option D:	score
5.	Targetted marketing, Recommended Systems, and Customer Segmentation are applications in which of the following
Option A:	Supervised Learning: Classification
Option B:	Unsupervised Learning: Clustering
Option C:	Unsupervised Learning: Regression
Option D:	Reinforcement Learning
6.	CART stands for…
Option A:	classification and regression tree
Option B:	choosing a regression task
Option C:	classification and regression task
Option D:	classification along regression task
7.	Naïve Bayes Algorithm is a ..... learning algorithm.
Option A:	Supervised
Option B:	Reinforcement
Option C:	Semi supervised
Option D:	Unsupervised

Paper code - 93775

8.	Which of the following can only be used when training data are linearly separable?
Option A:	linear hard-margin svm
Option B:	linear logistic regression
Option C:	linear soft margin svm
Option D:	the centroid method
9.	Impact of high variance on the training set ?
Option A:	depents upon the dataset
Option B:	underfitting
Option C:	both underfitting & overfitting
Option D:	overfitting
10.	What do you mean by a hard margin?
Option A:	The SVM allows very low error in classification
Option B:	The SVM allows very high error in classification
Option C:	The SVM allows no error in classification
Option D:	The SVM does not allow error in classification

Q2. (20 Marks Each)	**Solve any Two Questions out of Three** **10 marks each**
A	Explain the steps of developing Machine Learning applications in detail.
B	Explain regression line, scatter plot, error in prediction ; best fitting line.
C	Cluster the following eight points (with (x, y) representing locations) into three clusters: A1(2, 10), A2(2, 5), A3(8, 4), A4(5, 8), A5(7, 5), A6(6, 4), A7(1, 2), A8(4, 9) Initial cluster centers are: A1(2, 10), A4(5, 8) and A7(1, 2). The distance function between two points a = (x1, y1) and b = (x2, y2) is defined as- $d(a, b) = \|x2 - x1\| + \|y2 - y1\|$ Use K-Means Algorithm to find the three cluster centers after the one iteration
Q3. (20 Marks Each)	**Solve any Two Questions out of Three** **10 marks each**
A	Compare and contrast Linear and Logistic regressions with respect to their mechanisms of prediction.
B	Explain in detail PCA for dimension reduction.

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Paper code - 93775

C

Find complete linkage method of hierarchical clustering to find clusters of 5 data points with following distance matrix.

	1	2	3	4	5
1	0	9	3	6	11
2	9	0	7	5	10
3	3	7	0	9	2
4	6	5	9	0	8
5	11	10	2	8	0

Q4. (20 Marks Each)

Solve any Two Questions out of Three **10 marks each**

A

Explain K-mean clustering algorithm giving suitable example. Also, explain how K-mean clustering differs from hierarchical clustering.

B

What is support vector machine? What do you mean by support vectors, hyper plane and margin,support vectors?What will be the boundary for one dimensional data, two dimensional data and three dimensional data. Explain with suitable examples.

What is SVM? Explain the following terms: hyperplane, separating hyperplane, margin and support vectors with suitable example.

C

Create a decision tree using gini index to classify following dataset:-

Sr. No.	Income	Age	Own house
1	Very high	Young	Yes
2	High	Medium	Yes
3	Low	Young	No
4	High	Medium	Yes
5	Very high	Medium	Yes
6	Medium	Young	Yes
7	High	Old	Yes
8	Medium	Medium	No
9	Low	Medium	No
10	Low	Old	No
11	High	Young	Yes
12	Medium	Old	No

TE/ETRX/Sem-VI/C2019/May-2022

University of Mumbai

Examinations summer 2022

Paper Code: 93460

Time: 2 hour 30 minutes Embedded Systems & Real Time Operating Systems Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	---------- is a serial communication interface in Embedded system
Option A:	Bluetooth
Option B:	Cortex M3
Option C:	DMA controller
Option D:	ARM processor
2.	---------- Sensor is commonly used in Cruise control application.
Option A:	Thermal
Option B:	Heart rate
Option C:	Ultraviolet
Option D:	Proximity
3.	What does UML stand for?
Option A:	Universal model language
Option B:	Unified Modeling language
Option C:	Unit modeling language
Option D:	Unit model Line
4.	----------can be used as a embedded system core.
Option A:	ASIC
Option B:	DMA Controller IC
Option C:	USART IC
Option D:	RS - 232
5.	Which testing method is known as White Box testing?
Option A:	A method which uses white coloured box
Option B:	A method which needs check system code & behavior of internal structures.
Option C:	A method which does not check for errors.
Option D:	A method which tests the functionality of application, without peering into its internal structures or workings.
6.	One of the major drawbacks of assembly language programming over C is
Option A:	Higher memory requirements
Option B:	program executes faster
Option C:	Every processor has its own instruction set.
Option D:	hardware specific instructions are available
7.	----------is a time critical embedded real time system .
Option A:	Missile control
Option B:	Weather monitoring
Option C:	Coffee vending machine
Option D:	Washing machine
8.	Priority inversion is
Option A:	the condition in which a low priority task needs to wait for a high priority task

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Option B:	the condition in which a high priority task needs to wait for a low priority task
Option C:	the act of increasing the priority of a process .
Option D:	the act of decreasing the priority of a process dynamically
9.	Which one of the following embedded systems does not require an operating system?
Option A:	Air-craft control
Option B:	Car cruise control system
Option C:	Missile control
Option D:	Automatic Chocolate Vending machine
10.	_____is a key for resource sharing.
Option A:	Semaphore
Option B:	Pipes
Option C:	Context Switch
Option D:	Queue

Q2. (20 M)	**Solve any Two Questions out of Three** **10 marks each**
A	Draw and Explain with neat diagram waterfall model.
B	Discuss the significance of Low Power modes in Cortex -M3
C	Discuss Selection Criteria of Sensors & Actuators with example.

Q3. (20 M)	**Solve any Two Questions out of Three** **10 marks each**
A	What is the importance of Design metrics ? Which metrics are the most important in an embedded system? Support your answer with suitable diagrams and / or graphs.
B	Differentiate between Bluetooth & Zigbee communication interfaces.
C	How is Task Scheduling done in embedded system ? Explain Scheduling Algorithms.

Q4. (20 M)	**Solve any Two Questions out of Three** **10 marks each**
A	What is Multitasking ? Explain TCB , Task states with neat diagram.
B	Design FSM & discuss Case study for Washing Machine Embedded Application.
C	Explain Free RTOS Task Management , Event & Time management features .

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