TE / ETRX / SEM-VI / C-2019 / DEC. 2023

Duration: 3 Hours **Total Marks: 80**

Note:

1) **Question No 1 is Compulsory.**
2) **Answer any three from the remaining questions.**
3) **Assume suitable data wherever required**

Q1. Solve any four of the following. **(20)**

a. Explain Oxide related capacitances in MOSFET.
b. Write a short note on power dissipation in CMOS circuits.
c. Implement the function F= $\overline{(A+B+C).(DE)}$ using standard CMOS logic
d. Implement 4 X 4 NAND based ROM array.
e. Write short on High-speed adders.

Q2.a Explain Constant Voltage and Constant Field Scaling in detail with their advantages and disadvantages. **(10)**

b. Explain CMOS inverter characteristics mentioning all regions of operation. **(10)**

Q3.a Compare Pass transistor logic, NMOS logic and CMOS logic. **(10)**

b. Compare SRAM with DRAM. Draw 6T SRAM Cell and explain its read and write operations **(10)**

Q4.a Compare Static CMOS and Pseudo NMOS design styles. Implement 2 input NOR gate using pseudo NMOS design style. **(10)**

b. Calculate noise margin of a CMOS inverter with the given parameters: **(10)**
NMOS $V_{TO,n}$ =0.6V, u_nC_{ox} = 60 uA/V^2, (W/L)n = 8,
PMOS $V_{TO,p}$ = -0.7V, u_pC_{ox} = 25 uA/V^2, (W/L)p = 12,
V_{DD} = 3.3 V.

Q5.a Draw D flip flop using CMOS logic and explain the working. **(10)**

b. Draw Carry Look Ahead Adder chain using Dynamic CMOS Logic. **(10)**

Q6. Explain any four **(20)**

a. BJT and MOS Technologies
b. Noise Margin
c. Sense Amplifier
d. 4 X 4 Barrel Shifter
e. ZIPPER logic design style

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40584

Q.P. CODE

Paper / Subject Code: 37812 / Electromagnetic Engineering

TE/Sem-VII/ETRX/C-2019/Dec-2023

(3 hrs.) **Maximum Marks = 80**

NB:

1. Question No. 1 is compulsory and solve any THREE questions from remaining questions
2. Assume suitable data if necessary
3. Draw clean and neat diagrams

			Marks
Q1.		Answer the following:	
	a.	Derive an equation for Ampere Circuital Law.	5
	b.	What is Skin effect? Explain applications of Skin effect.	5
	c.	Define gain, bandwidth, HPBW and directivity with respect to antenna.	5
	d.	Explain boundary conditions of E and H fields for two media.	5
Q2.	A.	Find $\overline{D}$ at P(6,8,-10) caused by a) a point charge of 30mC at the origin b) a uniform line charge $\rho_L = 40\ \mu C/m$ on the z axis.	10
	B.	A uniform plane wave in a medium having $\sigma = 10^{-3}$ s/m, $\epsilon = 80\ \epsilon_0$ and $\mu = \mu_0$ is having frequency of 10kHz. Calculate- a) attenuation constant b) phase constant c) wave length d) velocity of wave.	10
Q3.	A.	Derive an expression for reflection and transmission coefficient for normal incidence in case of reflection from perfect dielectric.	10
	B.	Define polarization of a wave. Explain the types of polarization.	10
Q4.	A.	Derive expressions for electric and magnetic fields in far field region of an infinitesimal dipole.	10
	B.	Write a note on Smith chart and explain the steps to calculate SWR from the chart.	10
Q5.	A.	Write short notes on different EMI control techniques.	10
	B.	A lossless transmission line is 80 cm long and operates at a frequency of 600 MHz The line parameters are $L = 0.25\ \mu H/m$ and $C = 100$ pF/m. Find characteristic impedance, the phase constant and the phase velocity.	10
Q6.	A.	Starting with Maxwell's equation in differential form, explain the concept of displacement current.	10
	B.	Write short notes on sources and characteristics of EMI.	10

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G.P. code
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Duration: 3hrs **[Max Marks:80]**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Q1. Attempt any FOUR **[20]**

a Explain with example bit stuffing and byte stuffing in HDLC protocol. **[05]**

b Differentiate between IPv4 and IPv6. **[05]**

c Draw IPv4 header and explain its fields. **[05]**

d Differentiate between TCP and UDP protocol. **[05]**

e Explain Piggybacking in error control. **[05]**

Q2. a Explain CLOS non-blocking switching fabric with proper diagram. **[10]**
Sketch the three stage Space Division switch with N=18, group size of n=6, k=2. What is the condition required to make it non-blocking?

b Explain virtual circuit approach and datagram approach in packet switching. **[10]**

Q3. a Compare error control and flow control. **[05]**
Consider the use of 1000 bit frames on a 1 Mbps satellite channel with a 270ms delay. What is the maximum link utilization for **[05]**

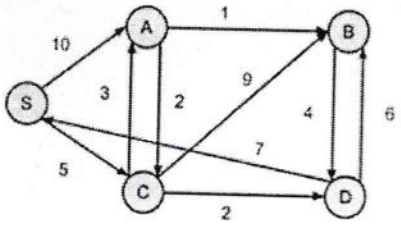
a. Stop-and-wait flow control?
b. Continuous flow control with a window size of 7?
c. Continuous flow control with a window size of 127?
d. Continuous flow control with a window size of 255?

b Explain the need for the nonpersistent, 1-persistent and p-persistent CSMA and their working with neat diagrams. **[10]**

Q4. a Explain the classful addressing in IPv4. **[05]**
An address in a block is given as 194.146.24.50/25. Find the subnet mask, number of addresses in the block, the first address, and the last address in the block **[05]**

p. code

b



[10]

Find and draw the shortest route from source node 's' to all other nodes using Dijkstra's and Bellman-Ford algorithm

Q5. a Discuss simple ALOHA and slotted ALOHA protocols with proper diagrams. Compare their throughput. **[10]**

b A is the primary station connected to the two secondary stations B and C in a half-duplex data transfer mode. Sketch the sequence of HDLC frames issued to implemented the data transfer for the following events: **[10]**

i) A sends a command to set up the NRM mode to B and C stations.
ii) The secondary stations B and C respond positively.
iii) A selects station C for initiating data transfer.
iv) C responds positively.
v) A sends frames 0, 1, 2, 3 to C and C acknowledges all the frames except 3.
vi) Station C sends positive acknowledgement for frame 3.

A sends a command to disconnect the data transfer mode and C acknowledges it properly.

Q6. a Explain domains and domain name space in DNS protocol. **[10]**

b Discuss the closed-loop congestion control mechanisms. **[10]**

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(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Solve **any 4**

(a) Compare I2C and CAN communication protocol. (5)

(b) Discuss difference between RISC and CISC cores. (5)

(c) Draw the diagram to explain various task states. (5)

(d) Examine the significance of Task Control Block. (5)

(e) Explain Hardware Software co-design in embedded systems. (5)

2. (a) Explain the following terms w.r.t Embedded systems: Code Density, Memory protection, power consumption and speed. (10)

(b) Draw architecture of the ARM Cortex-M3 and discuss its registers of all types. (10)

3. (a) Explain various types of testing used in embedded system design in detail. (10)

(b) Draw and explain Spiral model used in embedded product design life cycle (EDLC) (10)

4. (a) Elaborate all the functions of RTOS kernel. (10)

(b) Examine the low power modes in ARM CORTEX M3 (10)

5 (a) Discuss Semaphores and Mutex. Explain the functions to implement the same in any RTOS you know. (10)

(b) Decide whether the tasks are schedulable by Necessary and sufficient condition in an embedded system with 4 different tasks with task IDs T1, T2, T3, T4 and estimated completion time 12, 8,10,5 mS respectively. T1, T2, T3 and T4 have their cycle duration as 30, 40, 50 and 60 ms respectively. Schedule them by Rate Monotonic Scheduling method. (10)

6. (a) Explain the following FreeRTOS API functions xTaskCreate(), vTaskDelay(), vTaskGetInfo(), vTaskPrioritySet() (10)

(b) Design a suitable program model to design seat belt warning system for a four wheeler. (10)

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G.P. code.

43155

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(3 hours) **Total Marks: 80**

N.B.: (1) Question No 1 is Compulsory.

(2) Attempt any three questions out of the remaining five.

(3) All questions carry equal marks.

(4) Assume suitable data, if required and state it clearly.

Q.1. Attempt any **FOUR** **[20]**

A State any two properties of 2D-DFT.

B Derive High-Boost Filtered Image = (A-1) Original Image + High-Pass Image
Where, A is amplification factor

C Compare opening and closing.

D Define Inter-Pixel Redundancy. Explain with the help of an example.

E Write a note on image feature extraction.

Q. 2. **A** Define adjacency. Explain types of adjacencies with the help of an example. **[10]**

B What are various industrial applications of Machine Vision? Explain Machine Vision System for Quality Grading of Painted Slates in detail. **[10]**

Q. 3. **A** Find 2D-FFT of the following image. **[10]**

0	1	2	1
2	1	2	3
3	2	4	3
2	1	3	2

B Explain Huffman coding algorithm with the help of an example. **[10]**

Q.4. **A** Define the term image segmentation. Explain split and merge technique with the help of an example. **[10]**

B List different color models to represent a digital image. Explain color model used in display devices and printing devices in detail. **[10]**

G.P.code

Q. 5. **A** Define Histogram equalization. Explain the process of Histogram equalization. If we apply histogram equalization to the equalized image again how will the processed image look like. Show the equalized histogram after processing an equalized image. **[10]**

B For the following 4X4 image ,apply **[10]**

3	7	4	7
5	6	7	1
3	0	0	1
2	1	2	3

a. Digital negative

b. Thresholding

c. Contrast stretching (r1=2, r2=5, s1=1,s2=4)

Q.6. **A** What is Image Transform? What is the need for transform? What are the applications of transform. Prove whether DFT matrix is unitary and normalized. **[10]**

B If the arithmetic mean filter is applied to an image again and again what will be the resulting image? What will happen if we apply median filter to the same image? Explain with the help of an example. **[10]**

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Time: 3 hour **Max. Marks: 80**

Note: **1. Q.1 is Compulsory**

2. Solve any 3 out of Q.2 to Q.6

Q.1 Answer any four out of the following.(Each sub question carries 5 marks) **(20)**

a) Write a concurrent VHDL code for 4:1Multiplexer.

b) Explain Moore and Mealy type finite state machines general block diagram.

c) Explain Clock management in FPGA.

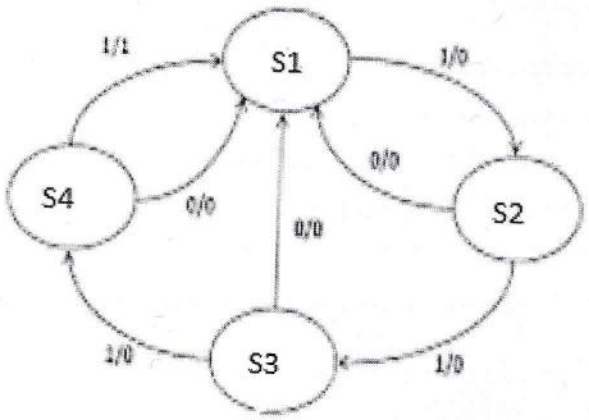
d) Differentiate between Signals and Variables in VHDL with suitable examples.

e) Reduce the following state transition table by identifying the equivalent states.

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
A	c	f	0	0
B	d	e	0	0
C	h	g	0	0
D	b	g	0	0
E	e	b	0	1
F	f	a	0	1
G	c	g	0	1
H	e	f	0	0

Q.2. A. Write a VHDL code for 8x8 ROM. (10)

Q.2. B. Write a VHDL code for the FSM whose state diagram is given below. (10)



G.P.code.

Q3. A. Write a VHDL code for 4 bit bidirectional shift register. (10)

Q3. B. Draw a state diagram of a finite state machine of Moore type that receives data bits serially at the serial input port S. The output Z which is normally Low, should become High for one clock pulse when a overlapping sequence 0-0-1-0 is detected at port S. Using minimum number of states design the circuit. (10)

Q4. A. i) Write a VHDL code for T flipflop. (05)

ii) Declare T flipflop as a component, and write structural code for 4 bit UP counter (05)

a

Q4. B. Explain the architecture of SRAM based FPGA. (10)

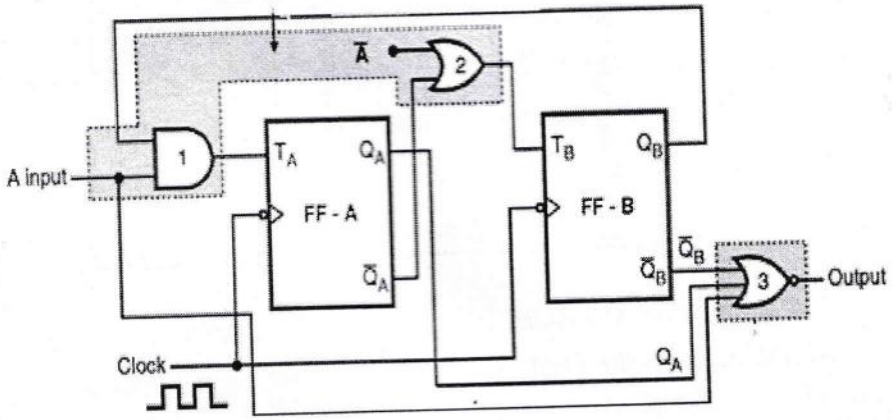
Q5. A. i) Explain the working of Serial adder.

ii)Write a VHDL code for the same. (10)

Q5. B. For the following state machine write:

i) Excitation equation ii) Next state equation iii) Output equation

iv) State transition/output table v) Draw the state diagram.



Q.6 A. Write a VHDL code for. Parallel multiplier (10)

Q.6 B. Write short notes on the following. (10)

i) Steps involved in digital design with FPGA

ii) Features and application of VHDL

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